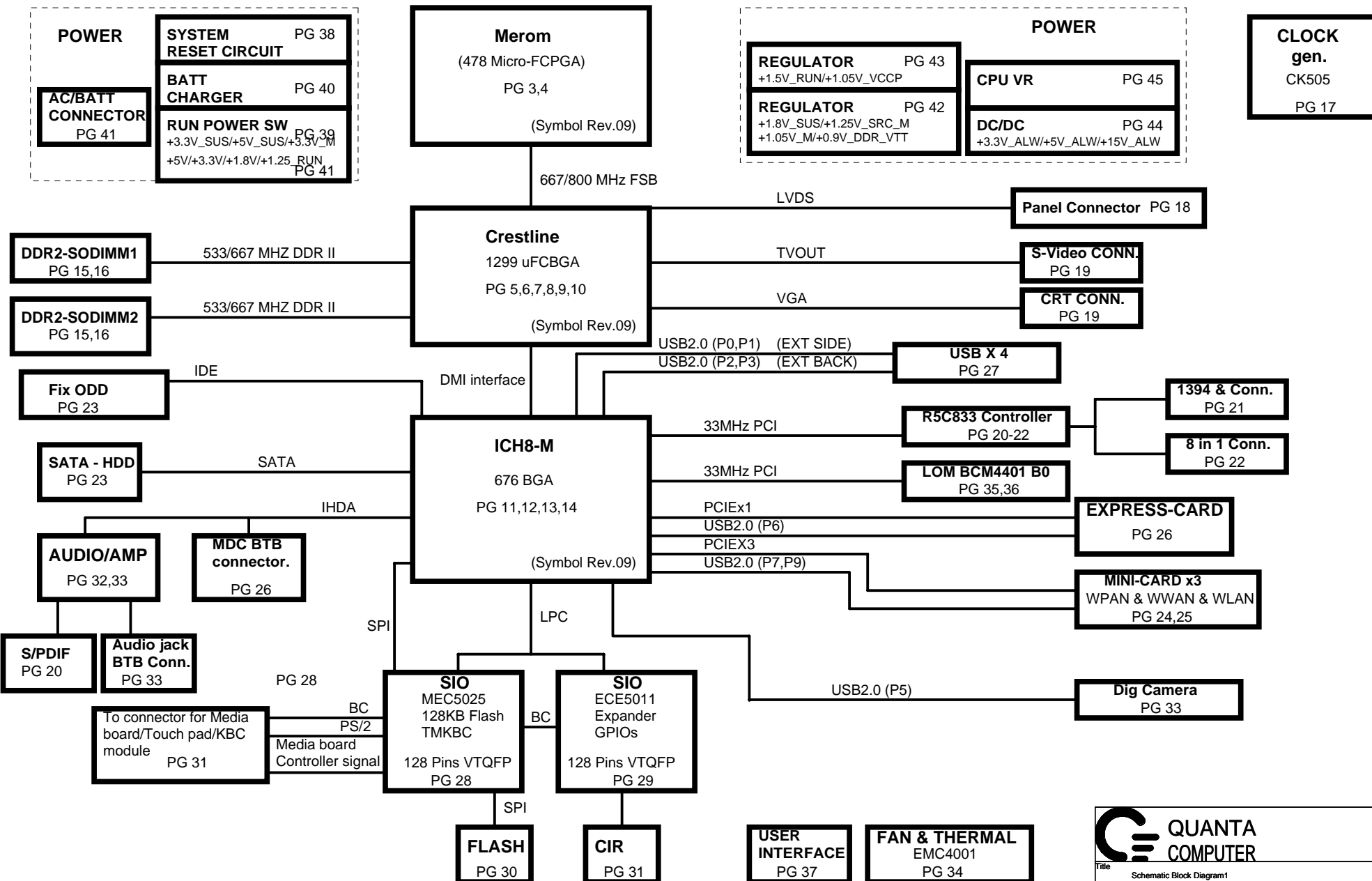


Cosica / Gilligan UMA

VER : 2B



Title		
Schematic Block Diagram1		
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INDEX

Pg#	Description	DNI LIST
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5-10	Crestline	
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15-16	DDRII SO-DIMM(200P)	
17	Clock Generator	
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20	8 in 1 controller	
21	1394 function	
22	8 in 1 connector	
23	SATA & IDE Conn	
24-25	Mini Card (WLAN/WPAN/WWAN)	
26	Express Card + MDC BTB Connector	
27	USB Conn.	
28	SIO (MEC5025)	
29	SIO (MEC5011)	
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40	Battery Charger	
41	DCIN/Batt Conn.	
42	1.25V,1.8V,0.9V	
43	1.5VSUS,1.05V(VTT)	
44	D/D Power	
45	CPU_ISL6260(3phase)	
46	EMI CAP & Screw Hole.	

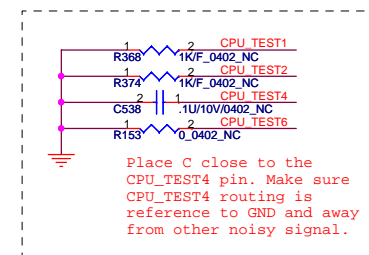
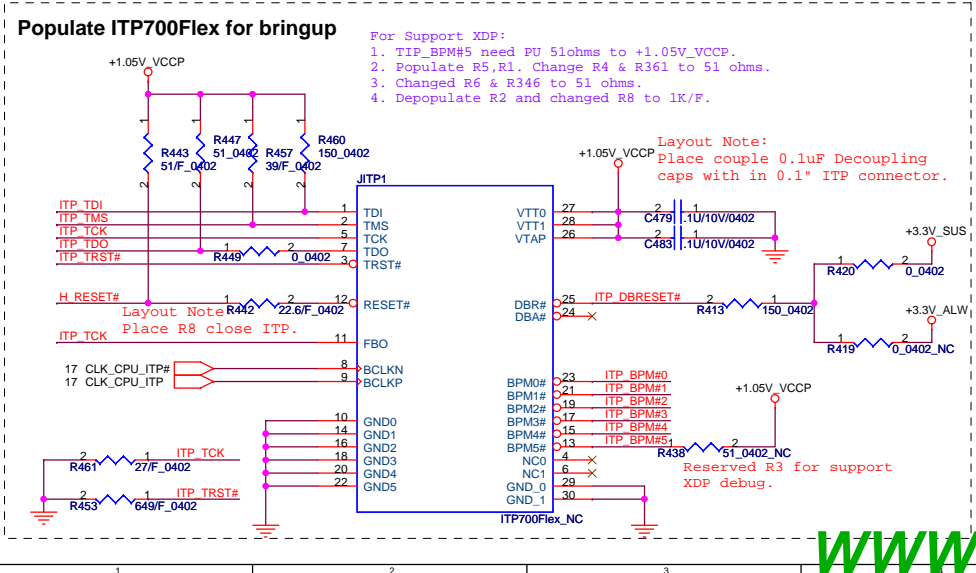
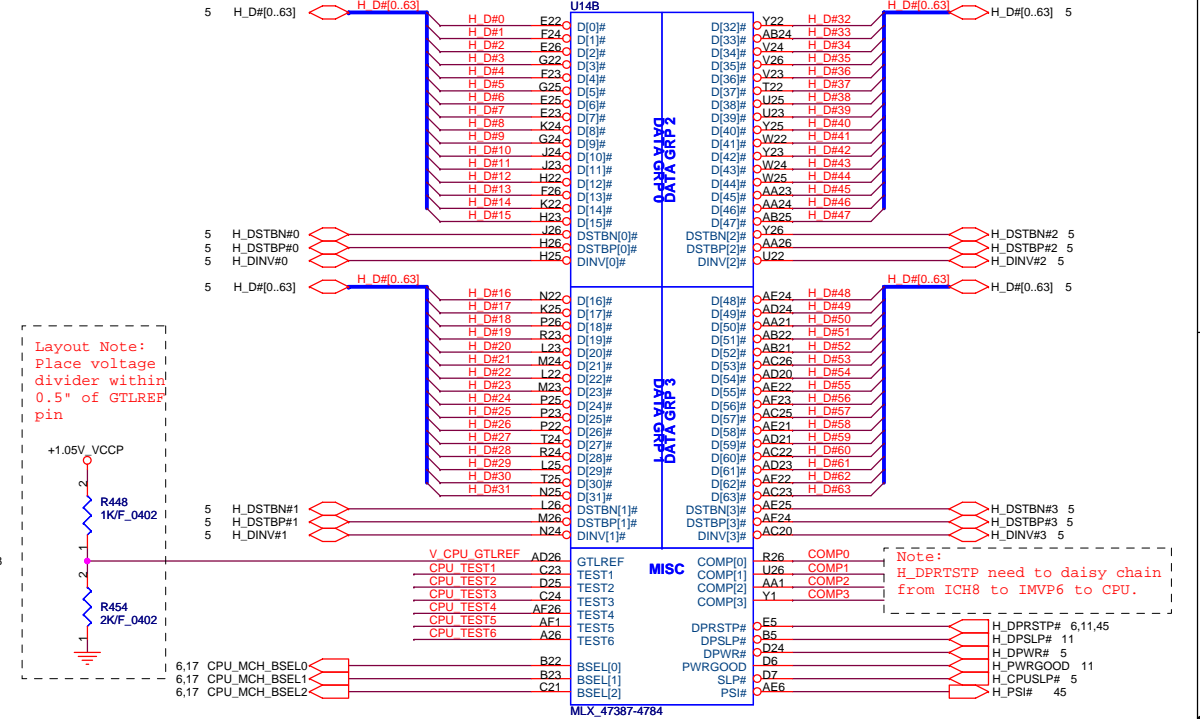
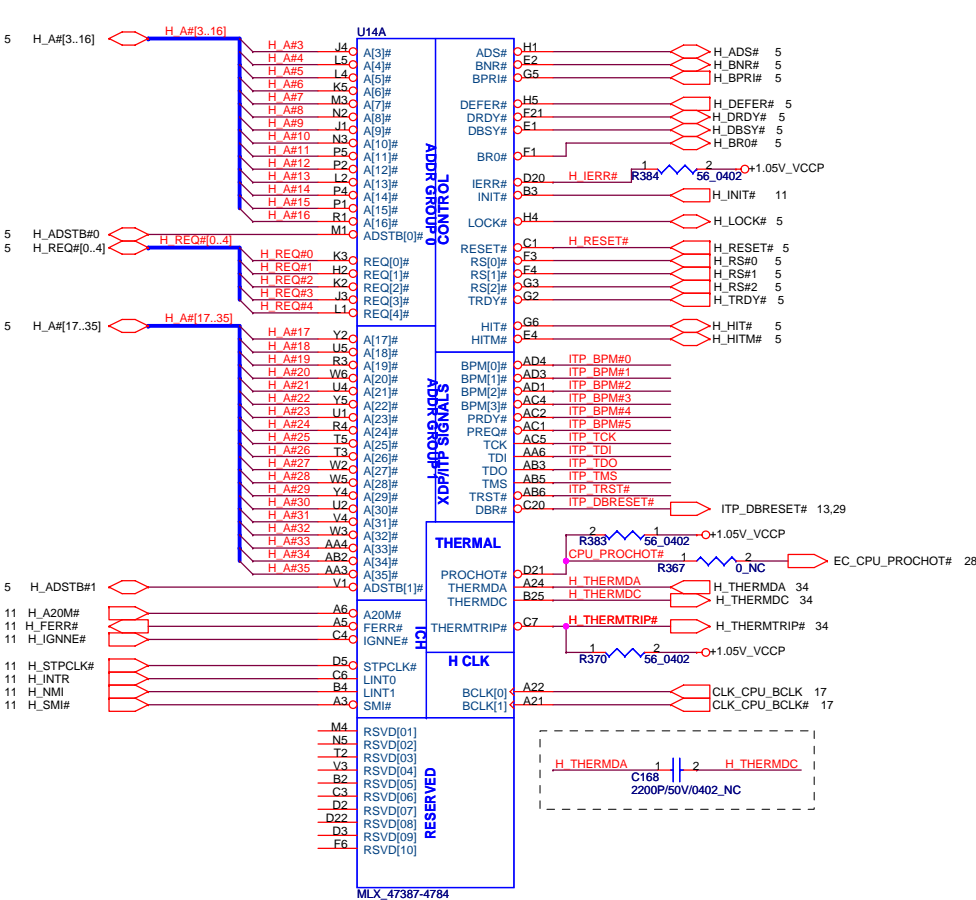
Power & Ground

Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (19V)	
PBATT+		MAIN BATTERY + (10~17V)	
PBATT+		SECOND BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~19V)	
RTC_PWR3_3V		RTC & +3.3V_RTC_LDO(3.3V)	
+VCC_CORE		CPU CORE POWER (1.5V)	RUNPWROK
+15V_ALW		LARGE POWER (15V)	SUS_ON
+3.3V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+3.3V_SUS		SLP_S5# CTRLD POWER	SUS_ENABLE
+3.3V_ALW		8051 POWER (3.3V)	ALWON/THERM_STP#
+5V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+5V_SUS		SLP_S5# CTRLD POWER	SUS_ON
+5V_HDD		HDD POWER (5V)	+5V_RUN
+5V_MOD		MODULE POWER (5V)	HDD_EN
+5V_ALW		LCD/CHARGE POWER (5V)	
+VDDA		AUDIO ANALOG POWER (5V)	AUDIO_AVDD_ON
+1.5V_RUN		CALISTOGA/ICH7 POWER	RUN_ON
+1.05V_VCCP		CPU/CALISTOGA/ICH7 POWER	RUN_ON
+1_8V_SUS		SODIMM POWER	SUSPWROK_5V
+1.8V_RUN		SDVO POWER	RUN_ON
+0.9V_DDR_VTT		SODIMM POWER	RUN_ON
+3.3V_LAN		LAN POWER	AUX_EN
 GND	ALL PAGES	DIGITAL GROUND	
 AGND_ISL6260		CPU GND	
 AGND_TPS51120		DC/DC POWER GND	
 AGND1		VTT POWER GND	
 AGND2		VTT POWER GND	
 8731AGND		CHARGER GND	



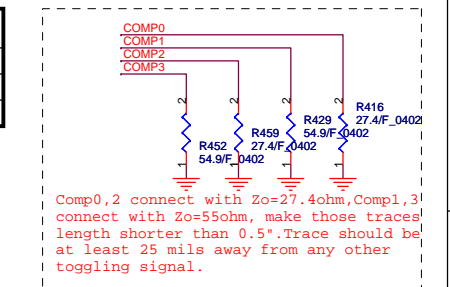
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For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0



ITP700 layout guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-down near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near ITP
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

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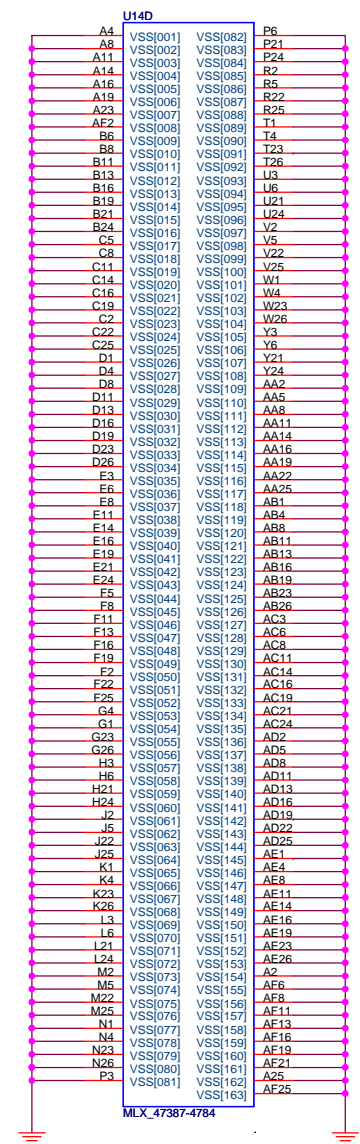
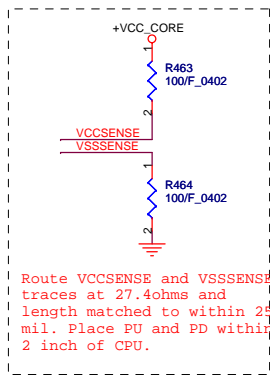
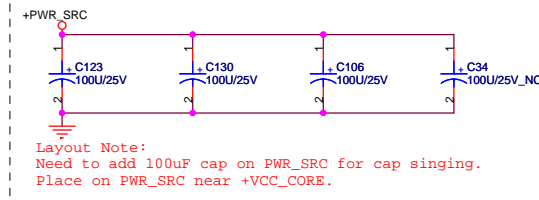
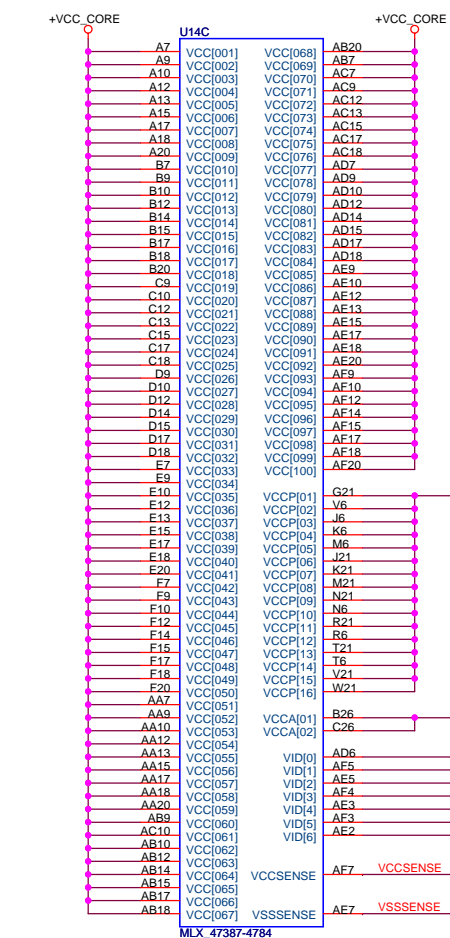
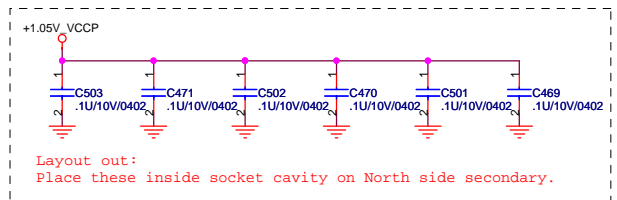
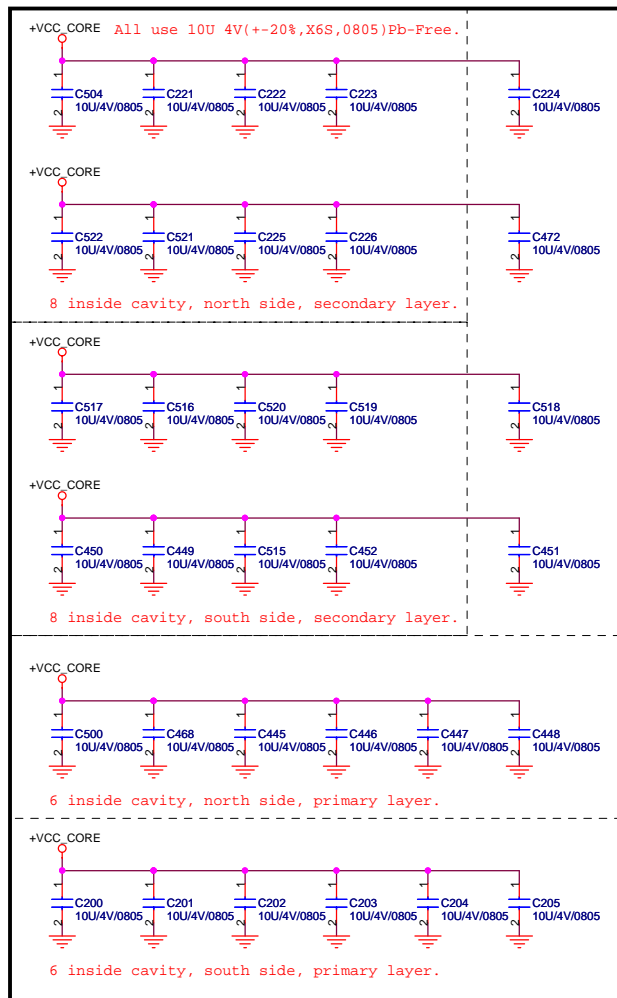
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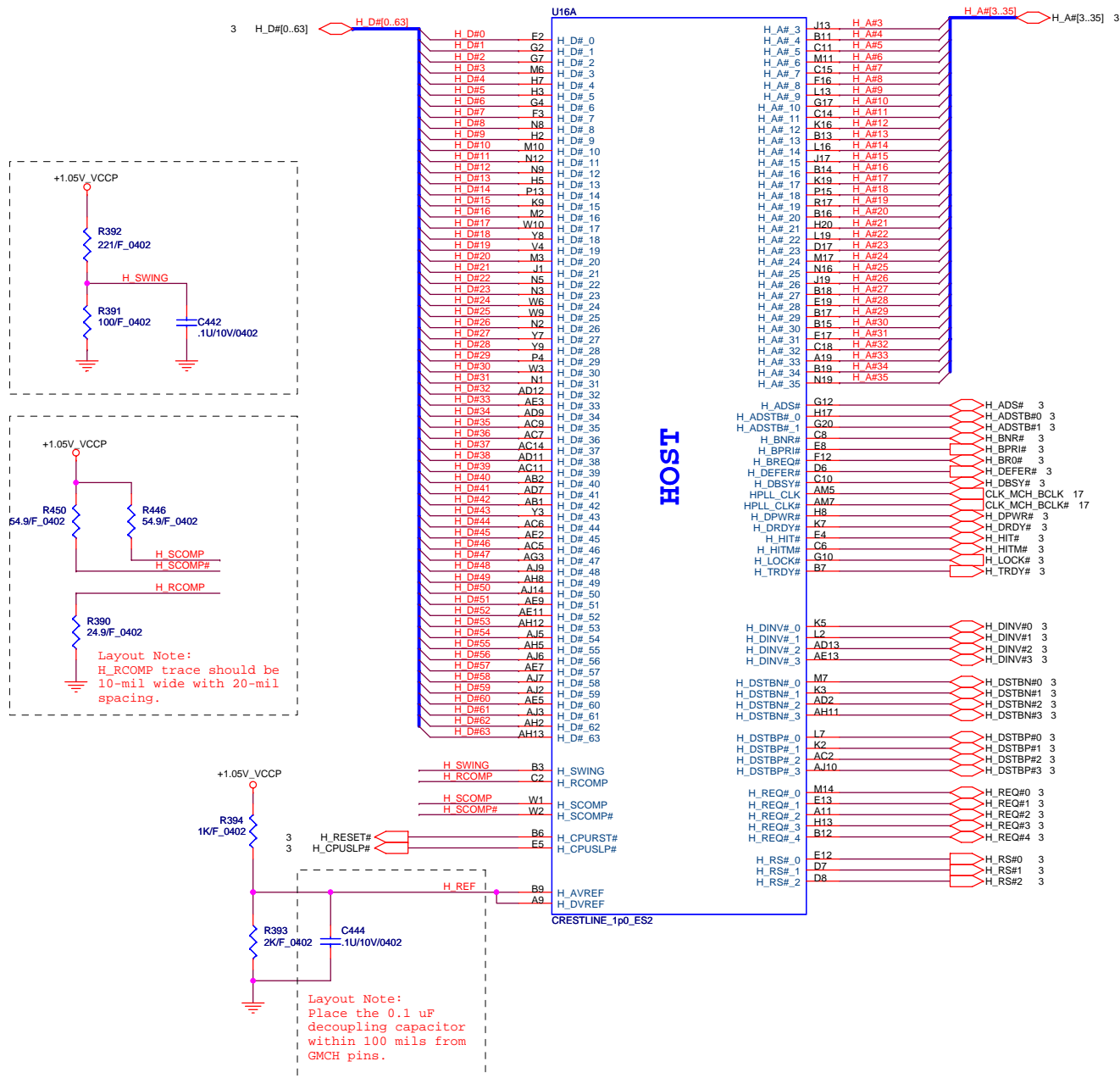
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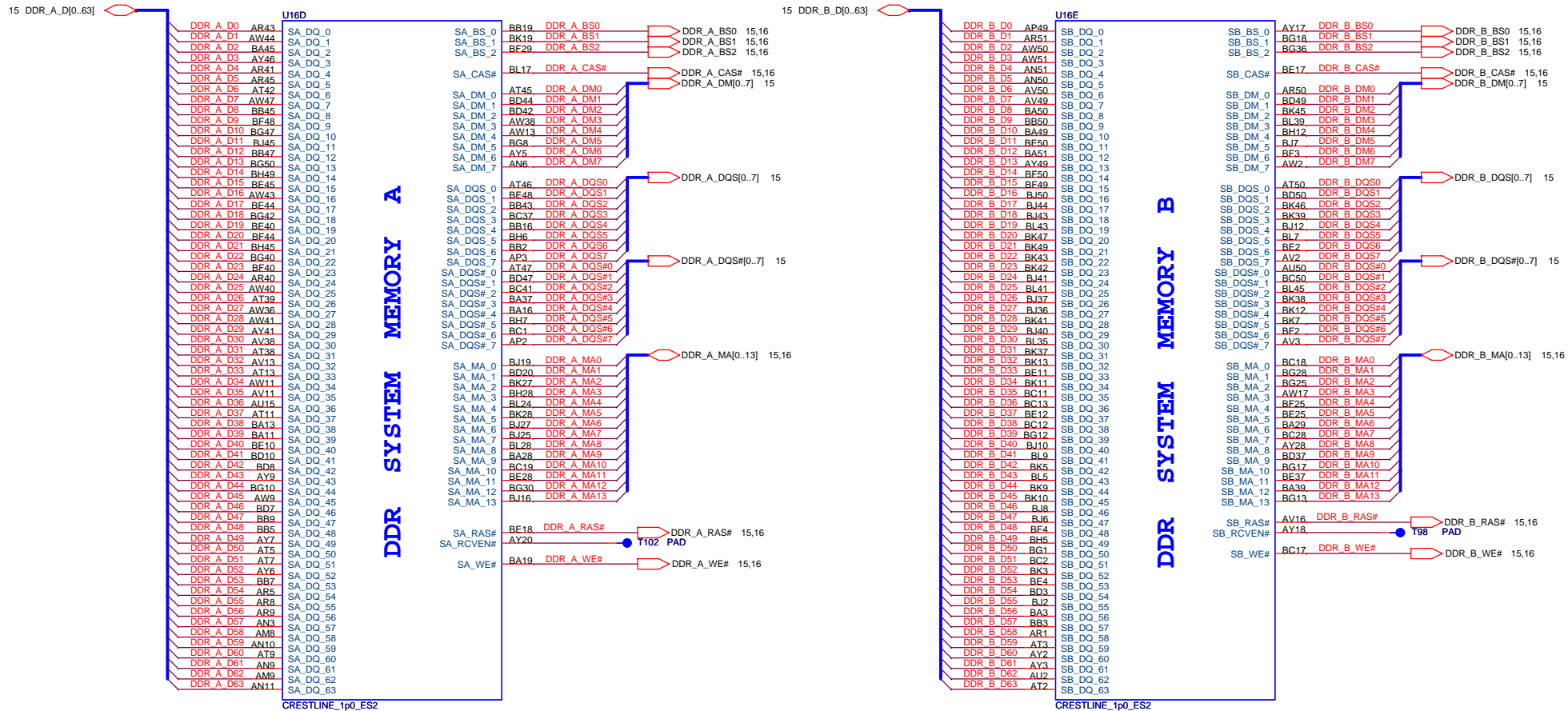
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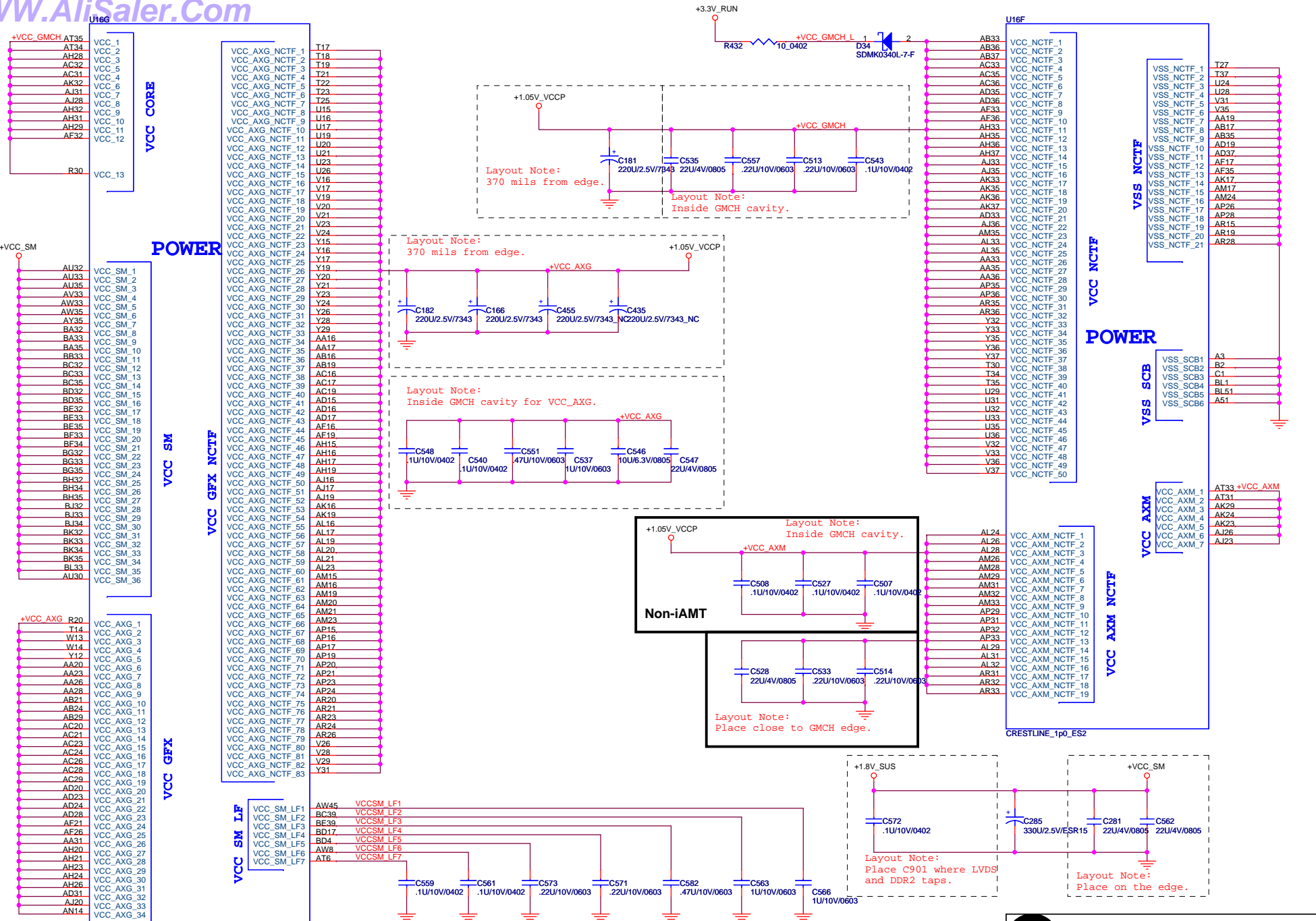
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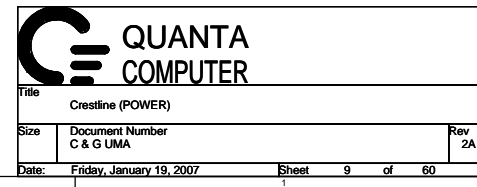
Rev 2A

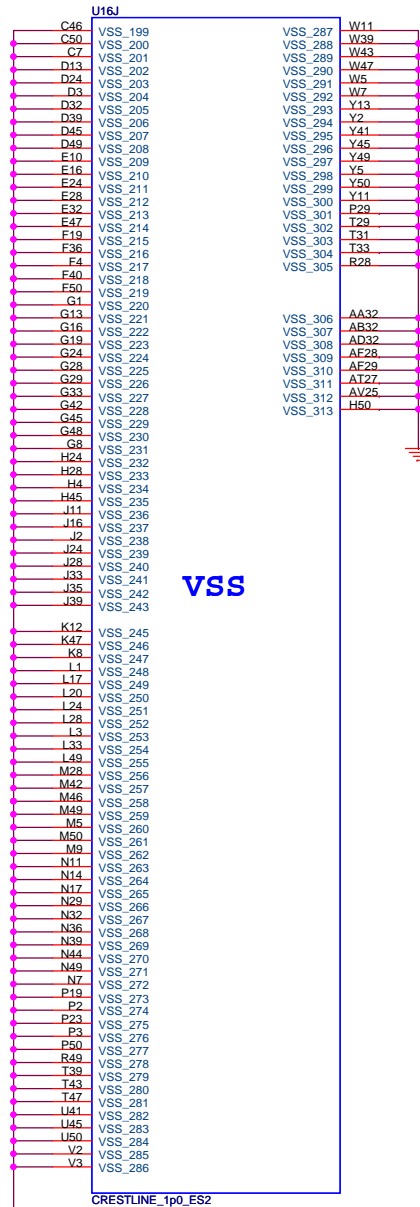
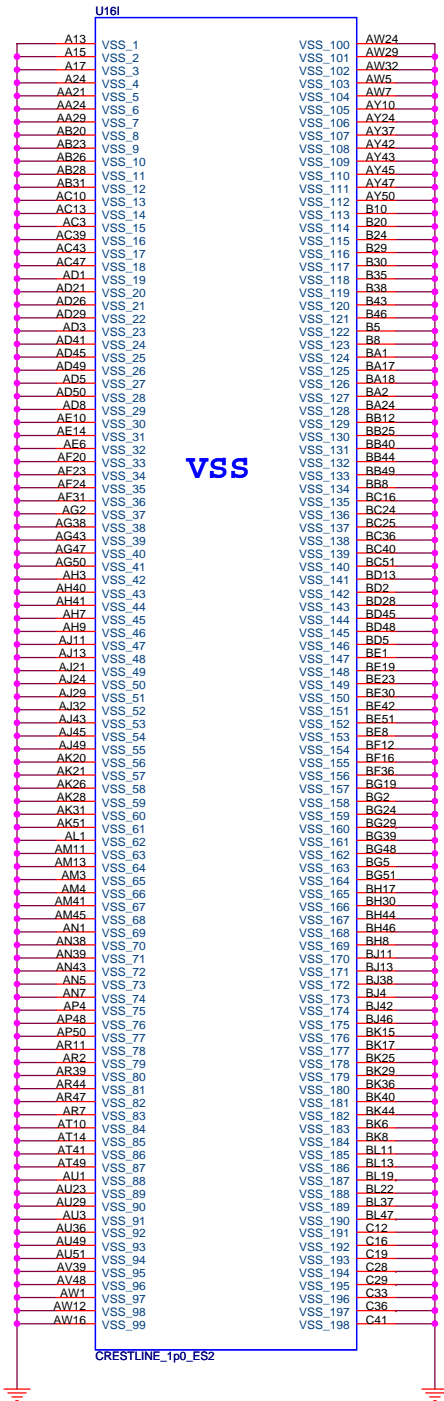





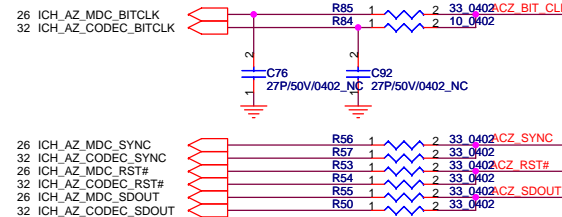
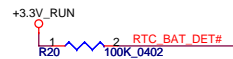
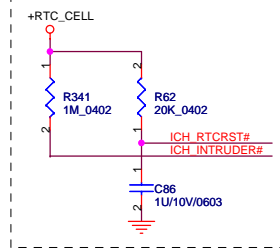
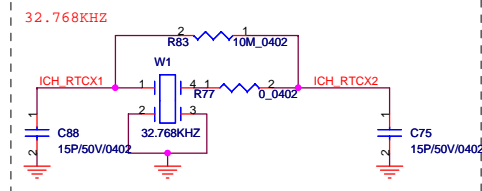




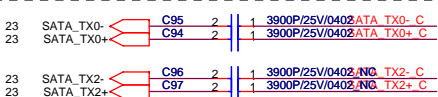




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Title Crestline (VSS)		
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Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R292, R286, R283 & R289 should equal distance to the T split trace point as R291, R285, R284 & R290 respective. Basically, keep the same distance from T for all series termination resistors.

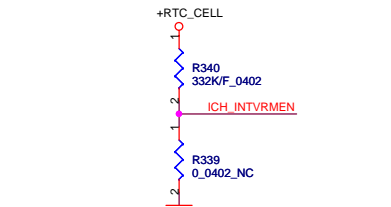


Populate C96, C97 (P/N:CH23904KB13) for Gilligan

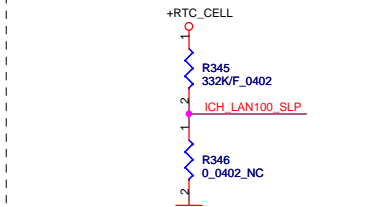
Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.

Place within 500mils of ICH8 ball

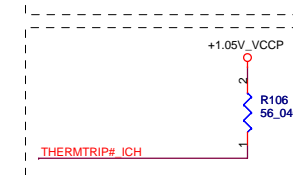
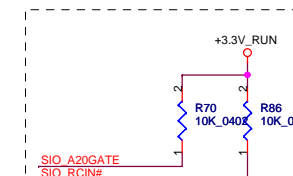
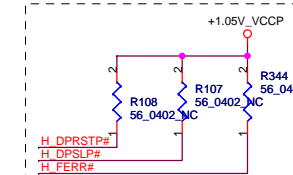
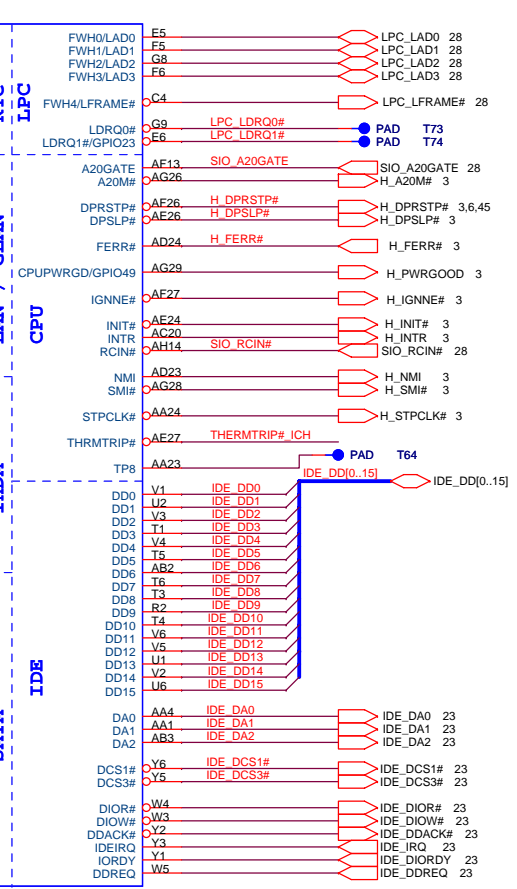
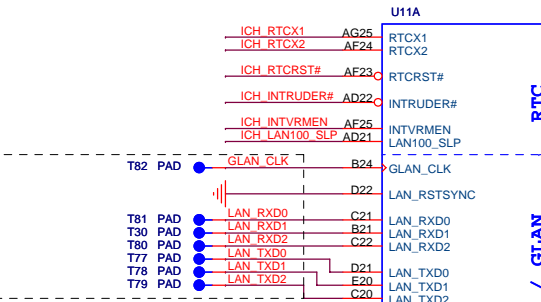
XOR Chain Entrance Strap		
ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)		
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)	



ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)		
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)	



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Title: ICH8-M (CPU,IDE,SATA,LPC,AC97,LAN)

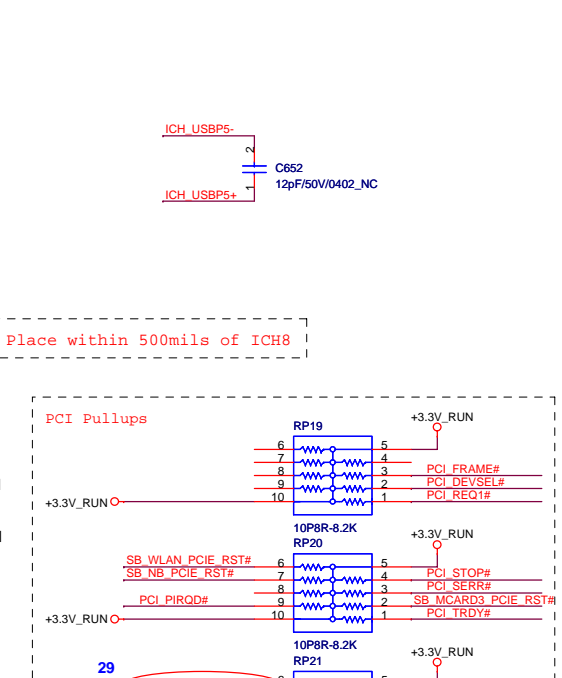
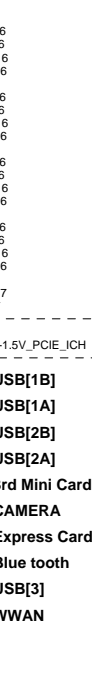
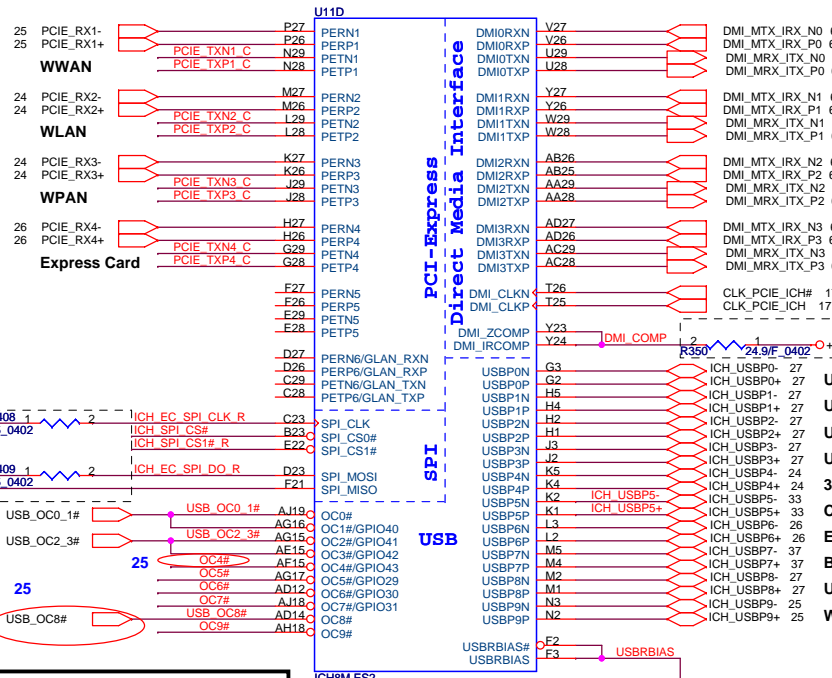
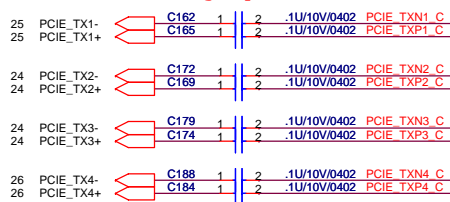
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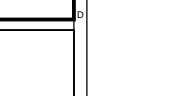
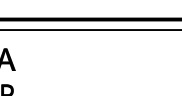
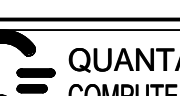
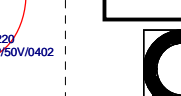
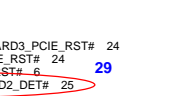
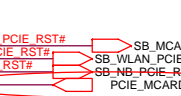
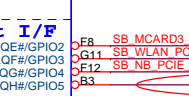
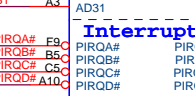
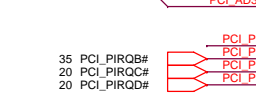
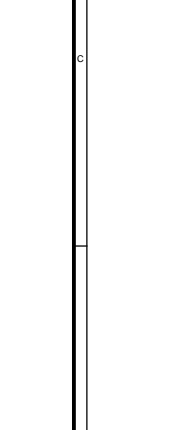
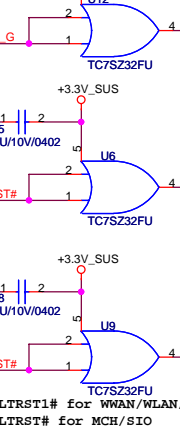
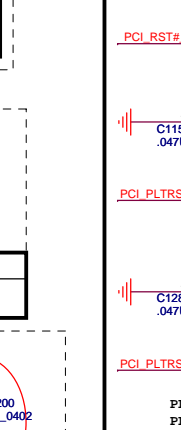
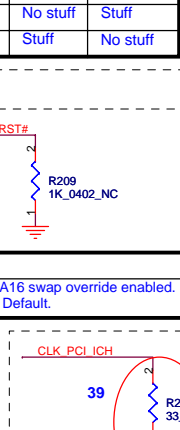
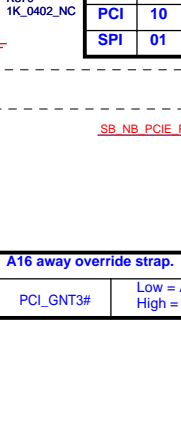
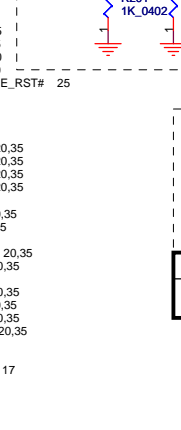
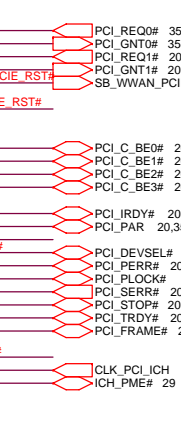
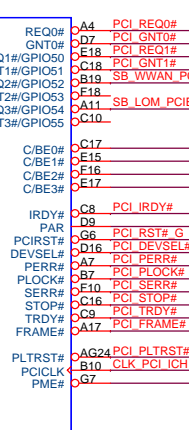
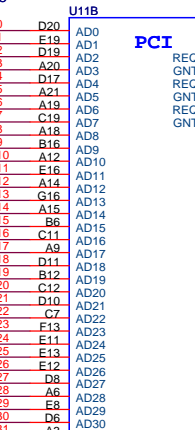
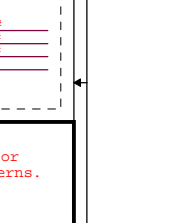
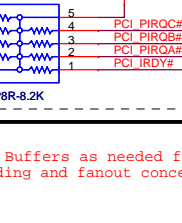
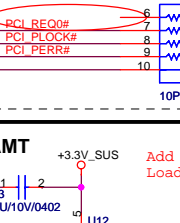
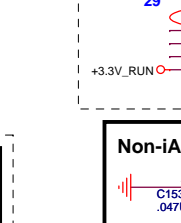
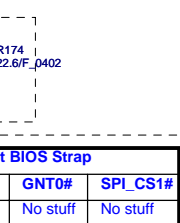
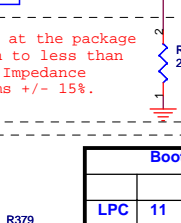
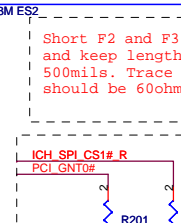
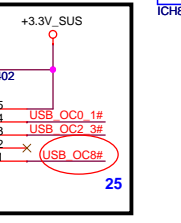
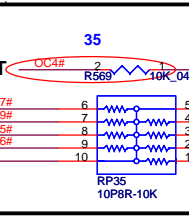
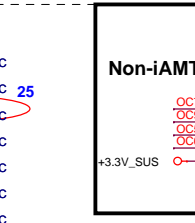
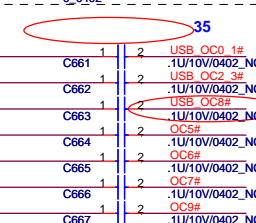
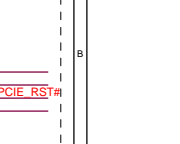
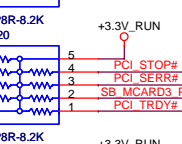
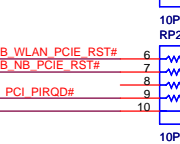
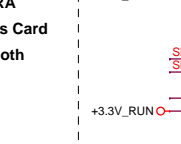
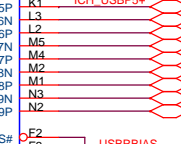
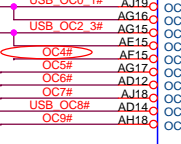
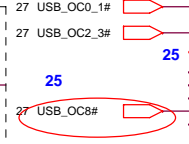
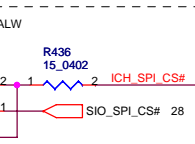
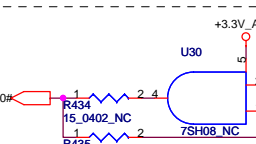
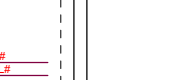
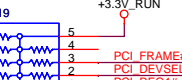
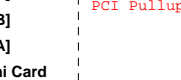
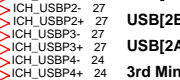
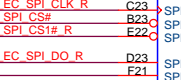
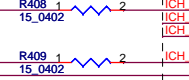
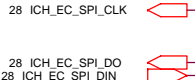
Sheet 11 of 60

Rev 2A

Place TX DC blocking caps close ICH8.



Layout Note:
Place R288, R688 and R282
within 500 mils from ICH.



PCI_PIRQB# for LOM
PCI_PIRQC# for Media Card
PCI_PIRQD# for 1394

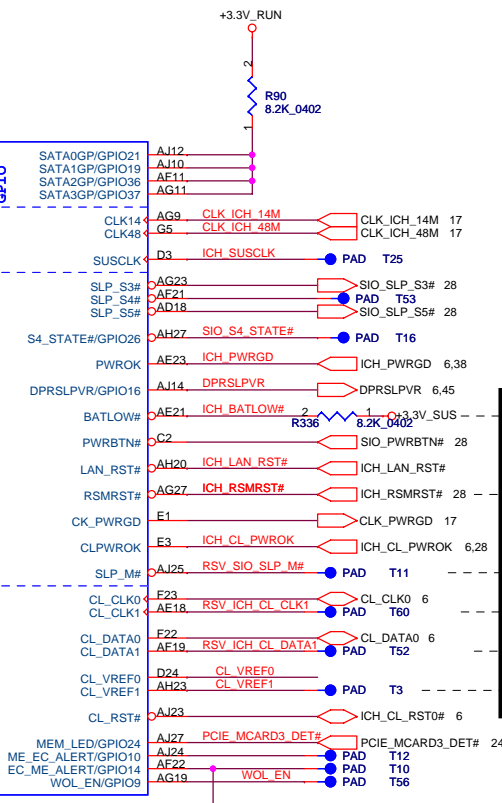
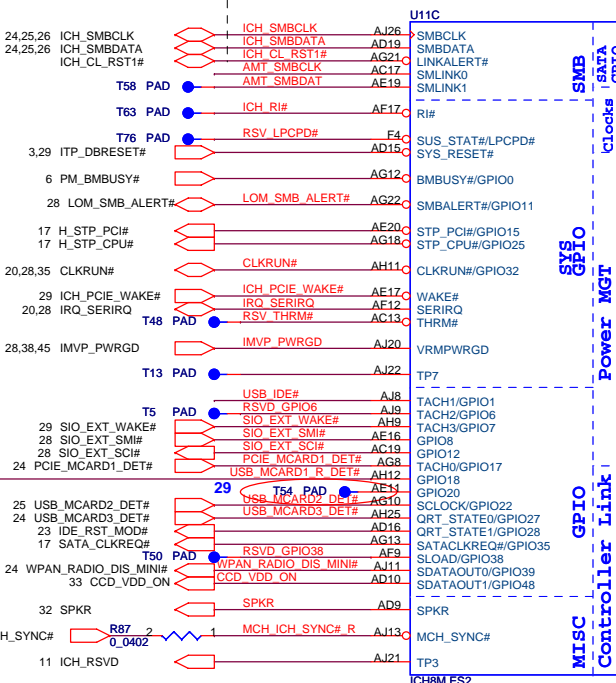
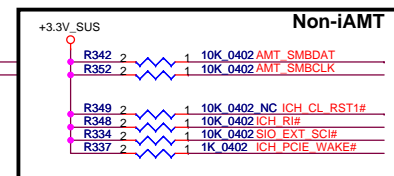
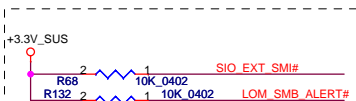
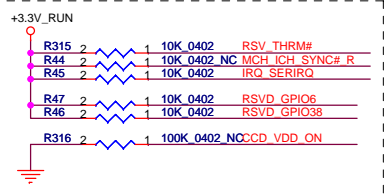
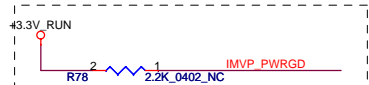
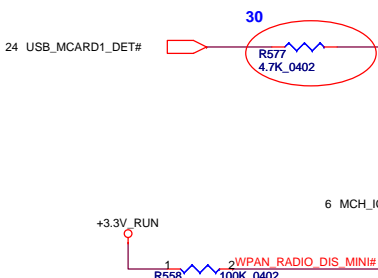
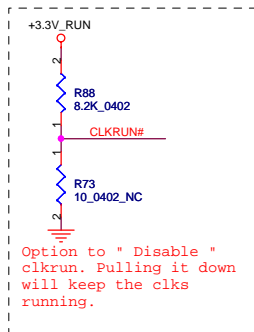
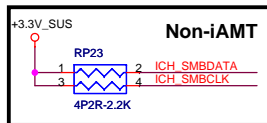
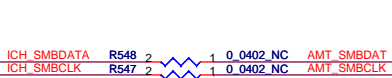
LOM	REQ0	GNT0	PIRQB
Card reader with 1394	REQ1	GNT1	PIRQC PIRQD

SB_LAN_PCIE_RST#	SB_WLAN_PCIE_RST#	SB_MCARD3_PCIE_RST#	SB_NB_PCIE_RST#
R207	R202	R372	R203
R208	R202	R208	R208

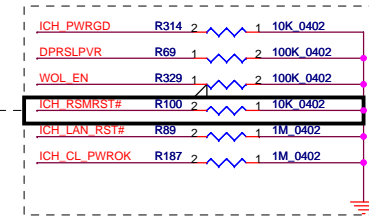
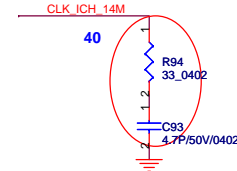
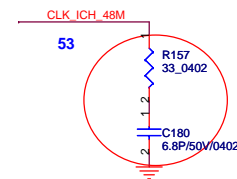
SB_LAN_PCIE_RST#	SB_WLAN_PCIE_RST#	SB_MCARD3_PCIE_RST#	SB_NB_PCIE_RST#
R207	R202	R372	R203
R208	R202	R208	R208

SB_LAN_PCIE_RST#	SB_WLAN_PCIE_RST#	SB_MCARD3_PCIE_RST#	SB_NB_PCIE_RST#
R207	R202	R372	R203
R208	R202	R208	R208

SB_LAN_PCIE_RST#	SB_WLAN_PCIE_RST#	SB_MCARD3_PCIE_RST#	SB_NB_PCIE_RST#
R207	R202	R372	R203
R208	R202	R208	R208



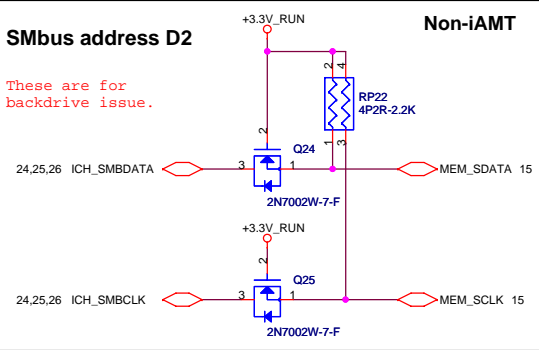
Place these close to ICH7.



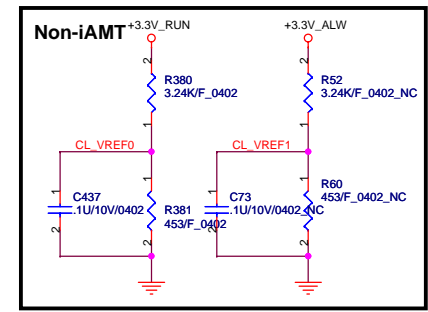
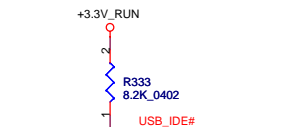
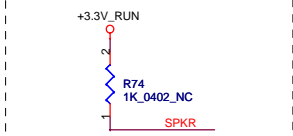
Non-iAMT

SMbus address D2

These are for backdrive issue.



No Reboot strap.
SPKR Low = Default. High = No Reboot.

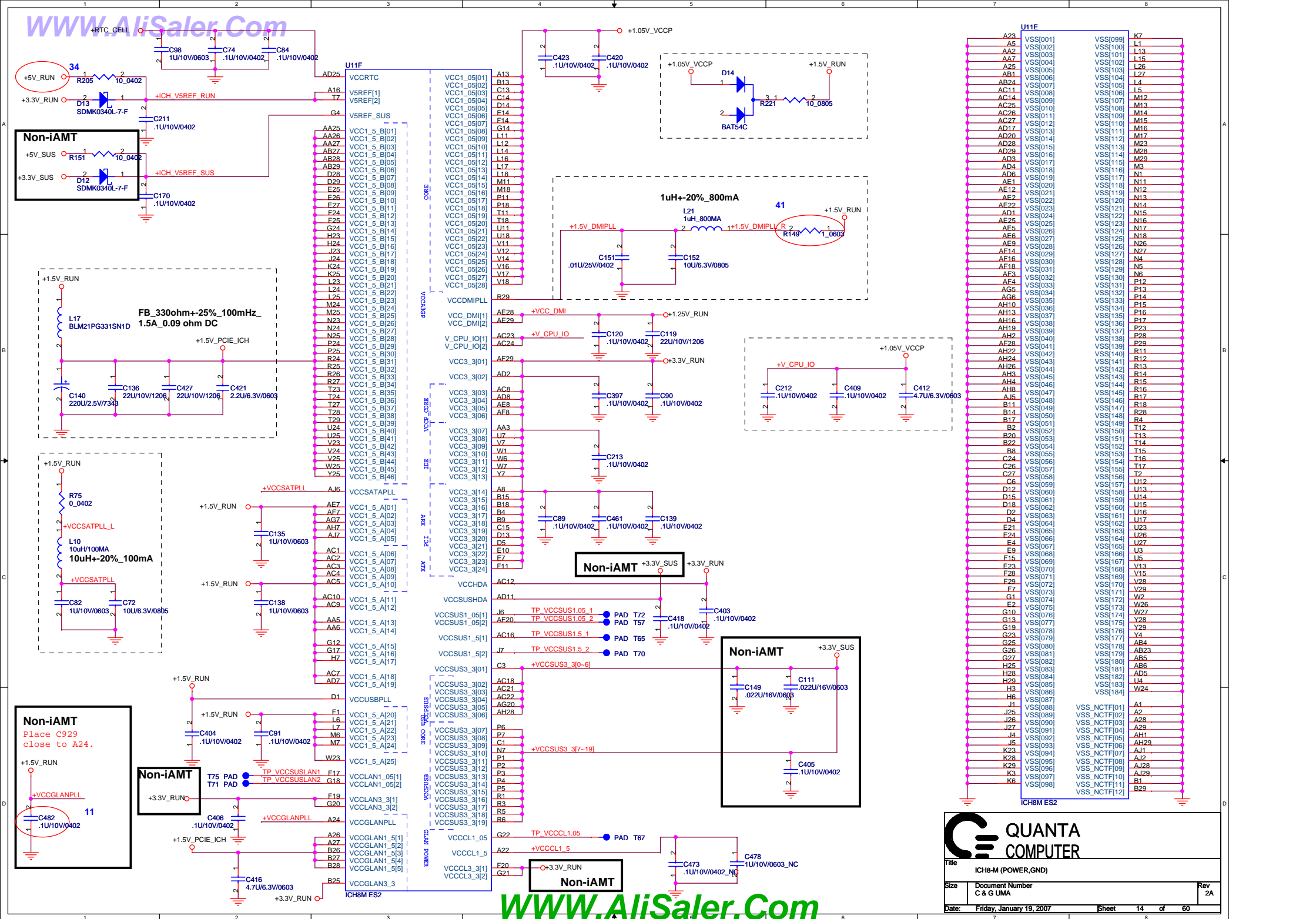


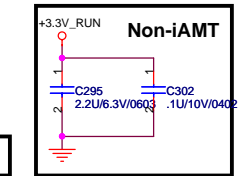
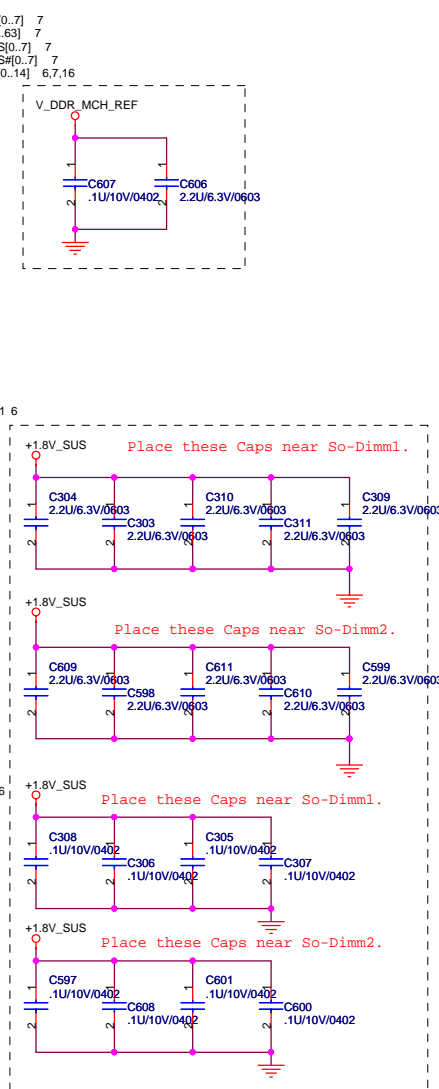
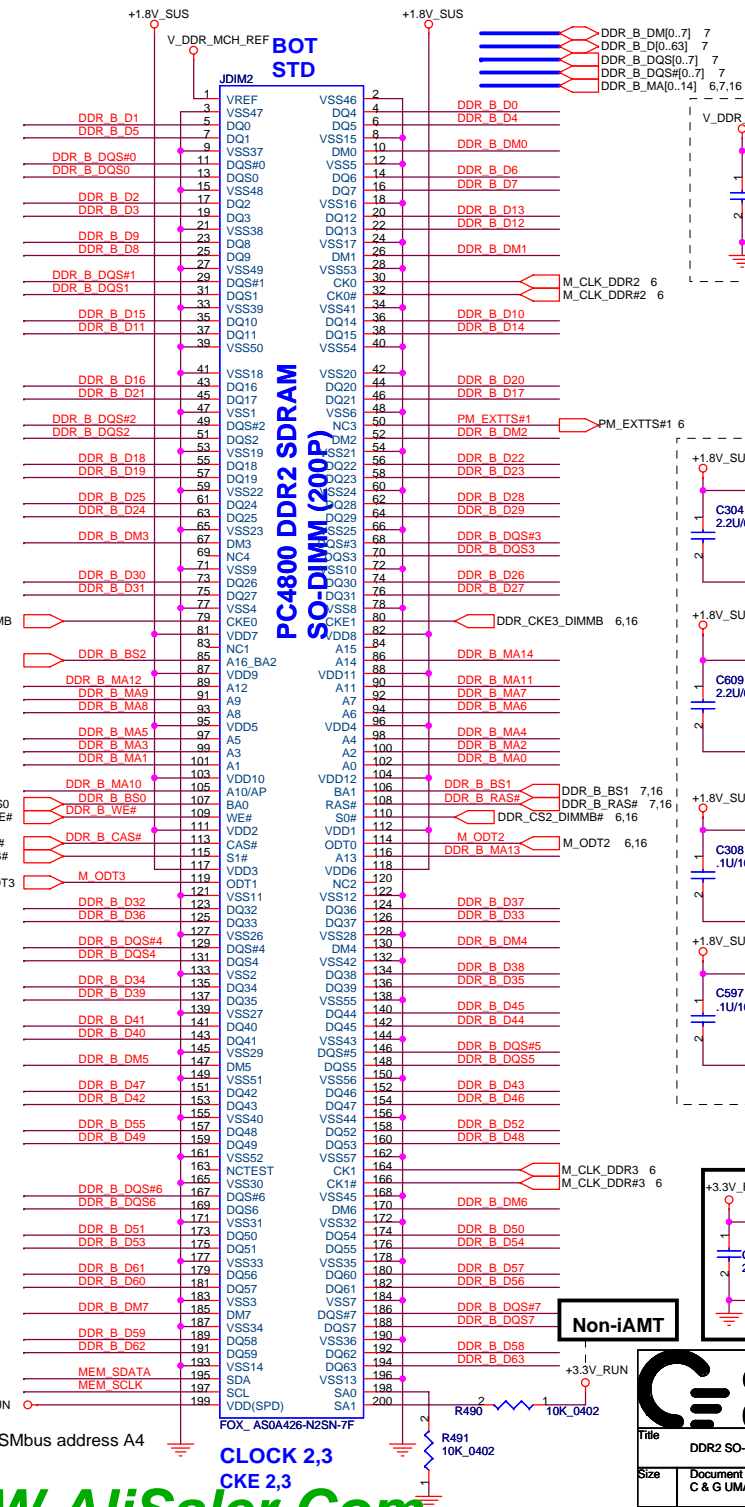
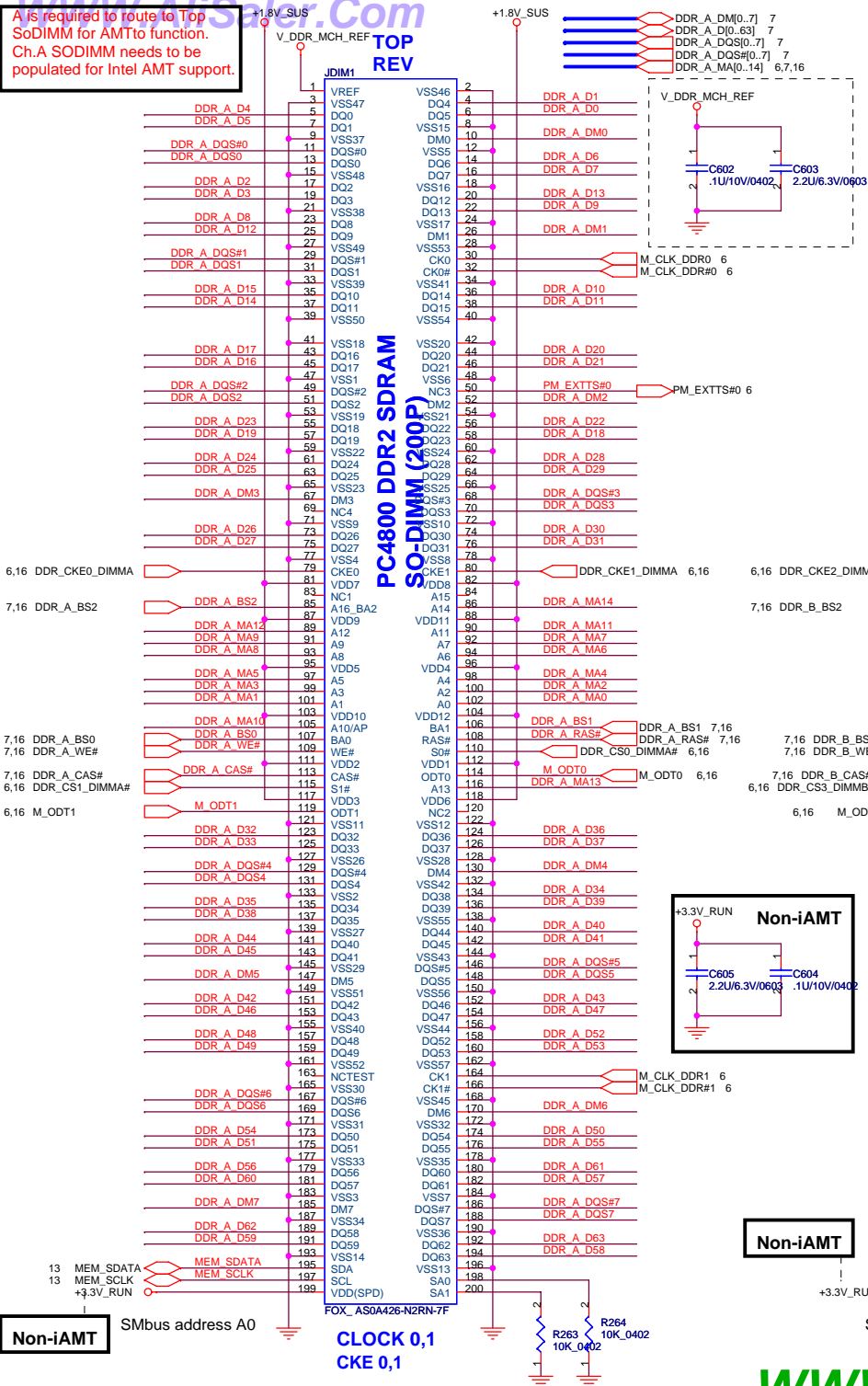
QUANTA COMPUTER

Title: ICH8-M (PM,GPIO,SMB,CL)

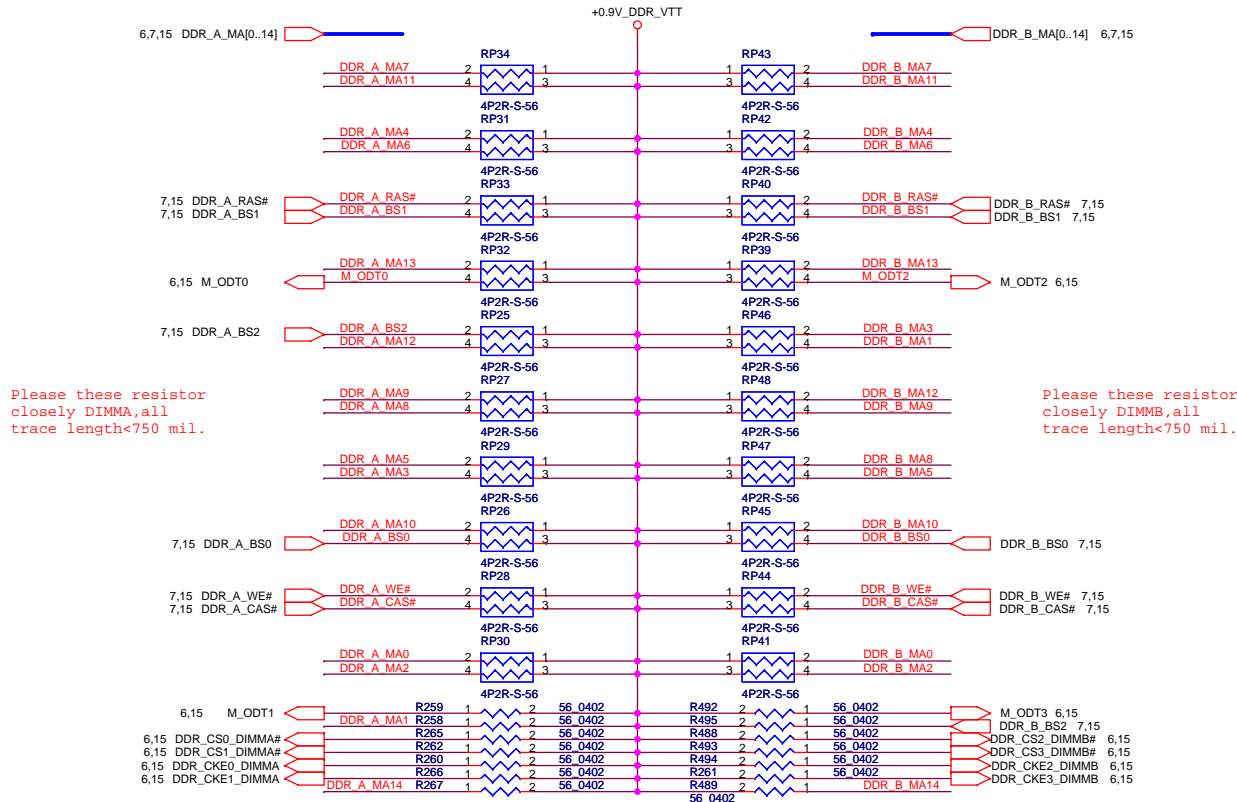
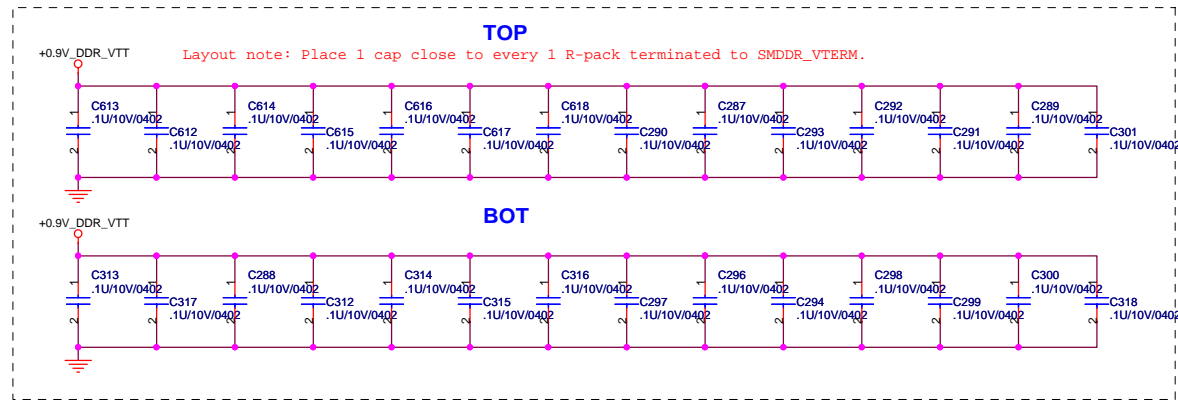
Size: Document Number C & G UMA Rev 2A

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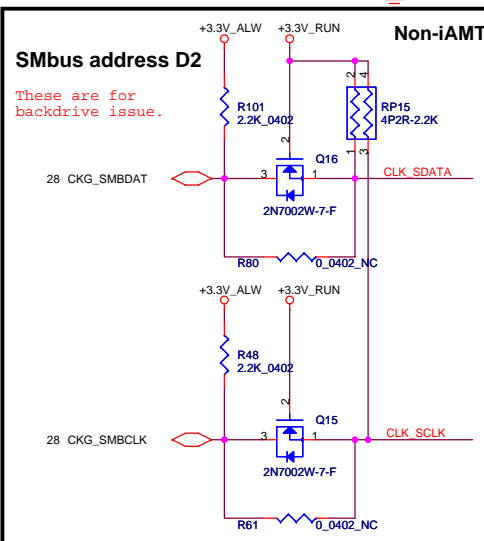
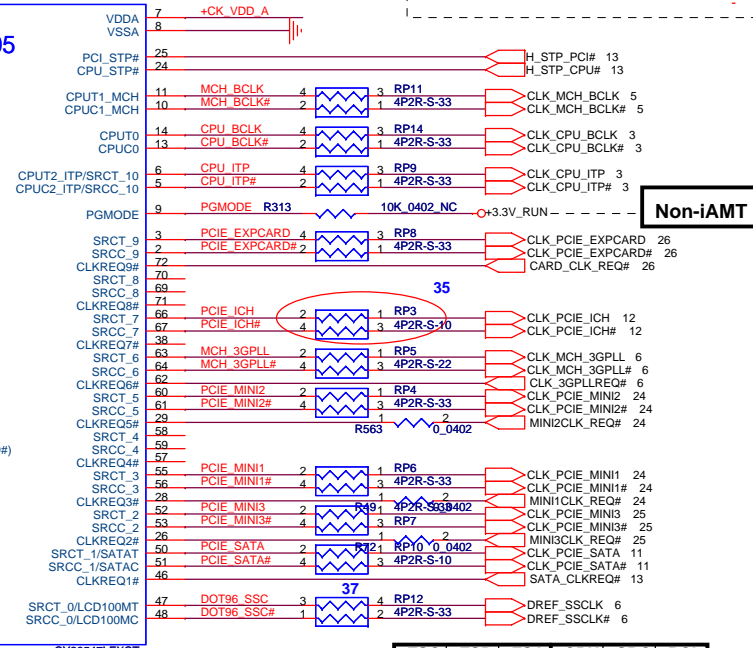
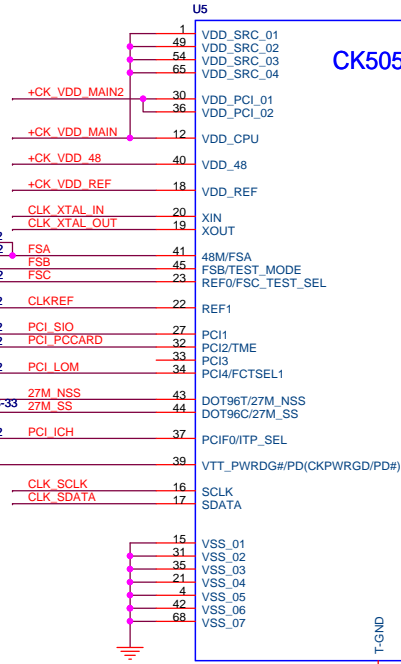
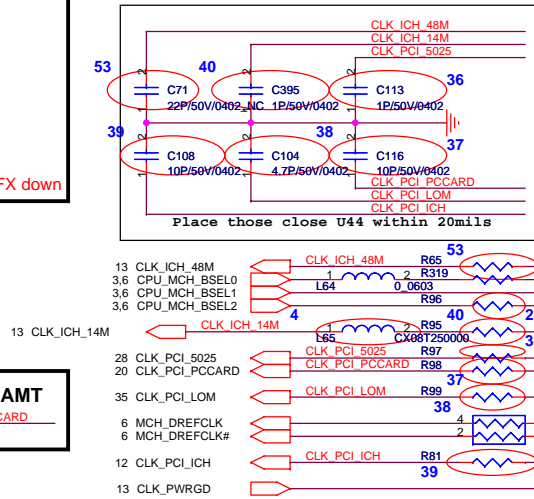
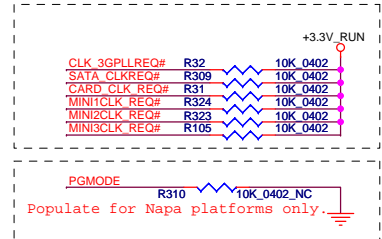
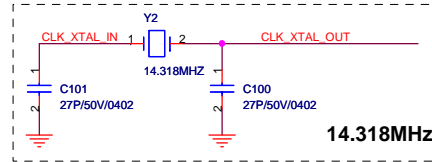
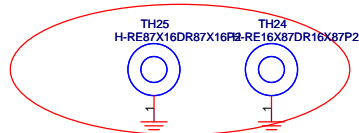
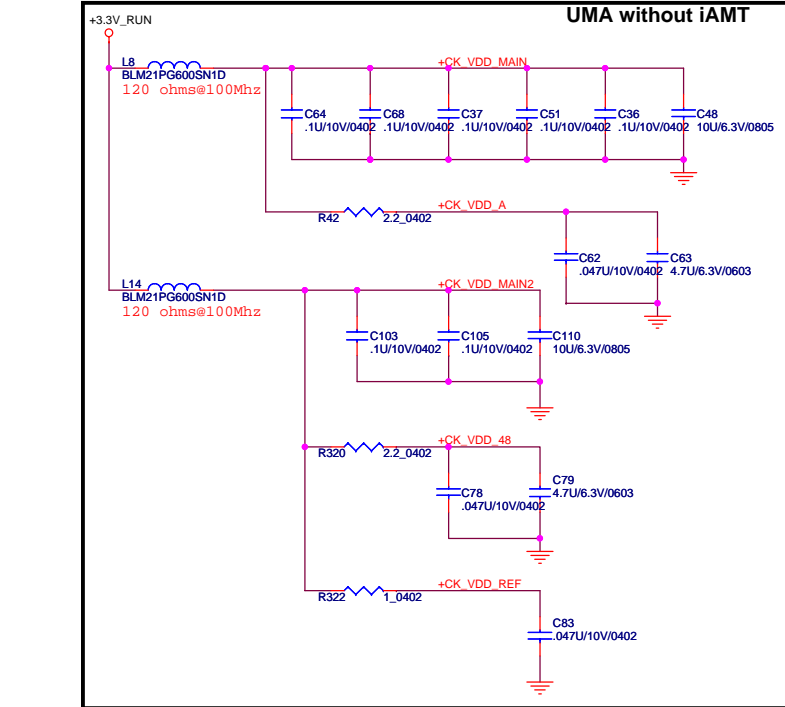
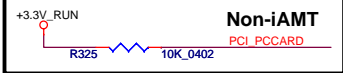
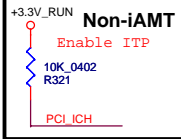
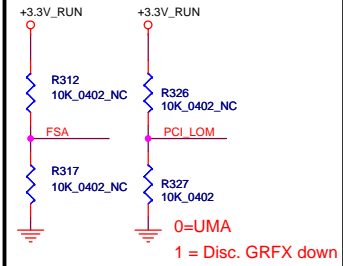


Title				DDR2 SO-DIMM (200P) X 2			
Size		Document Number C & G UMA				Rev 2A	
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Title: DDR2 RES ARRAY		
Size:	Document Number: C & G UMA	Rev: 2A
Date: Friday, January 19, 2007	Sheet: 16	of 60

Non-iAMT



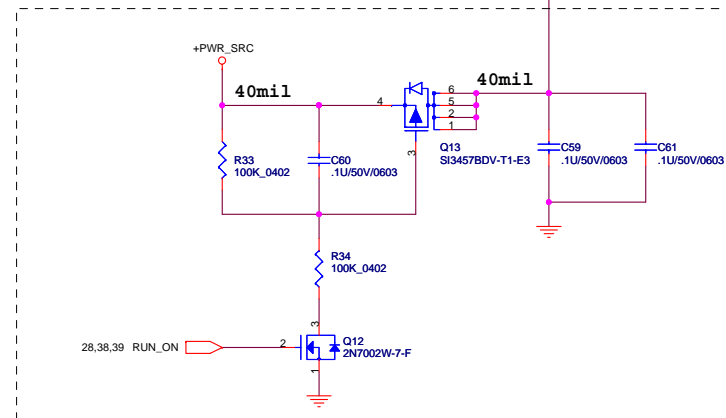
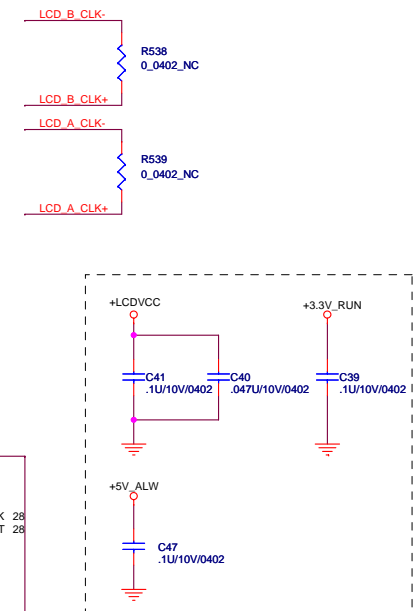
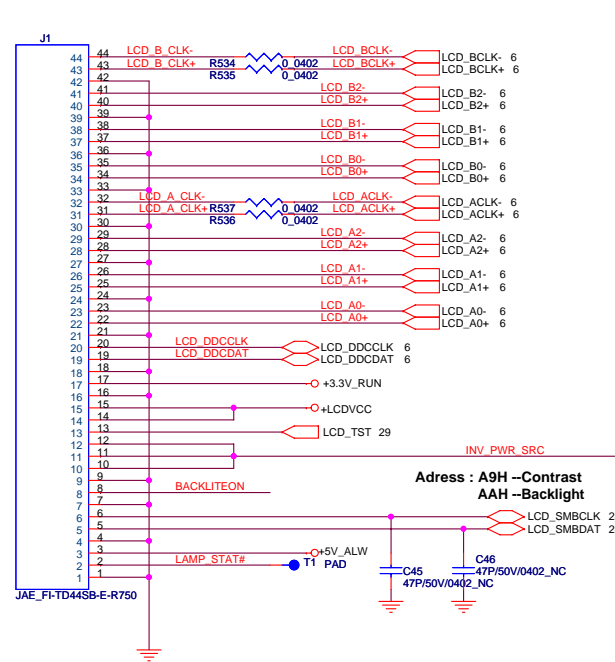
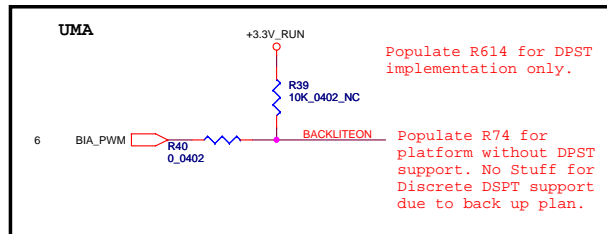
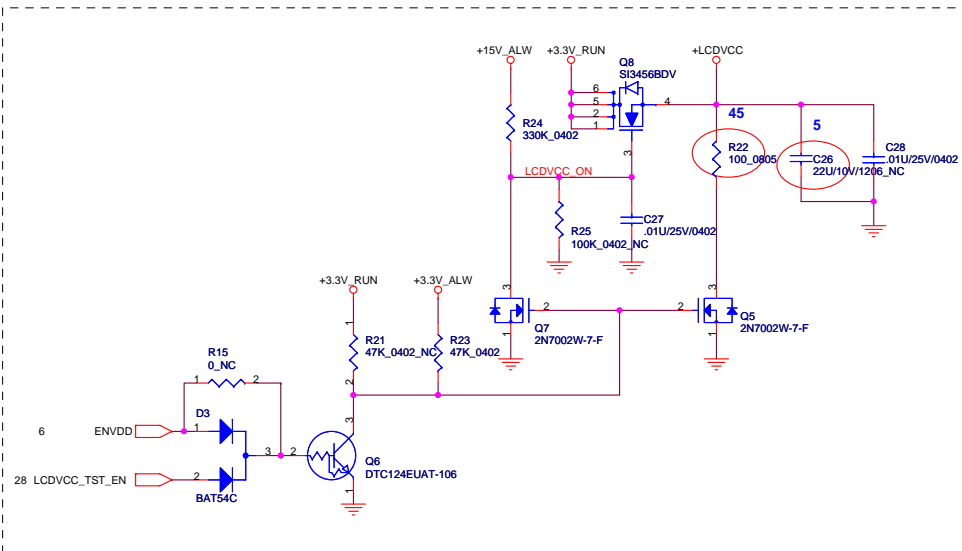
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM = FCTSEL1

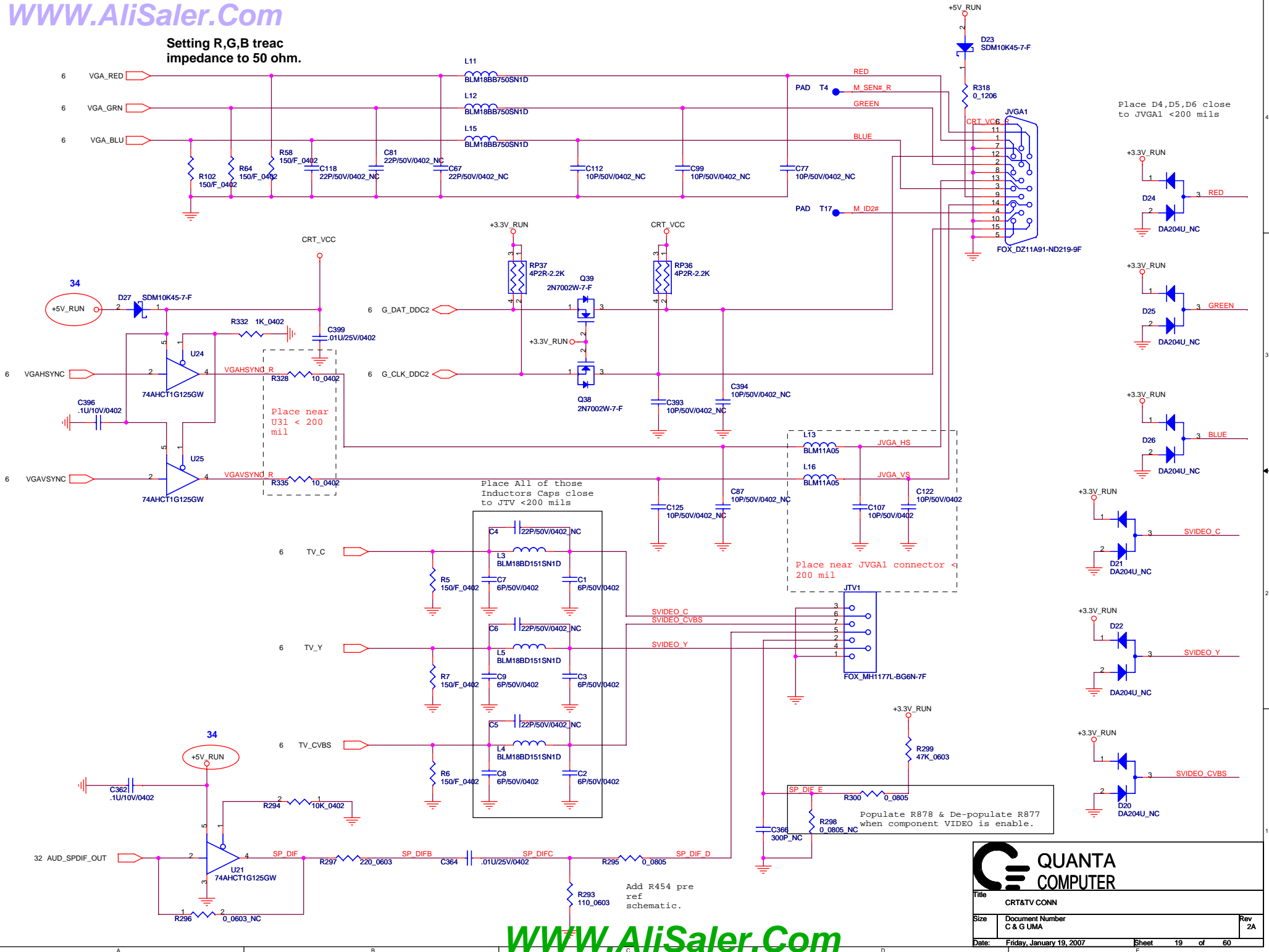
FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0



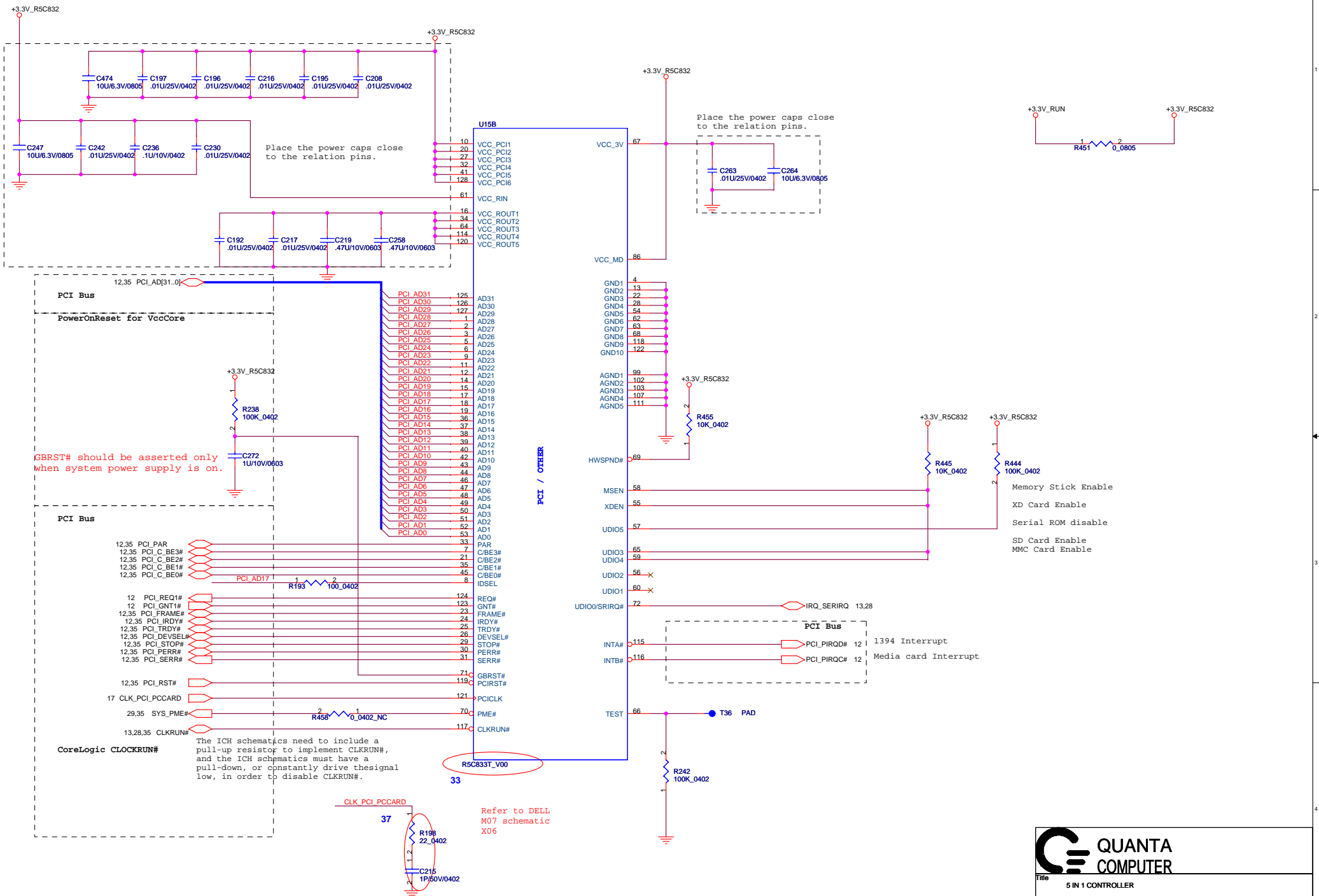
Title			
CLOCK GENERATOR			
Size	Document Number	Rev	
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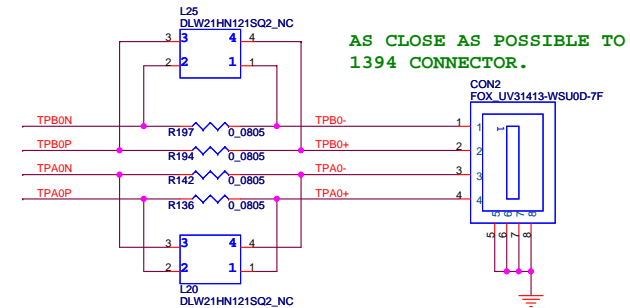
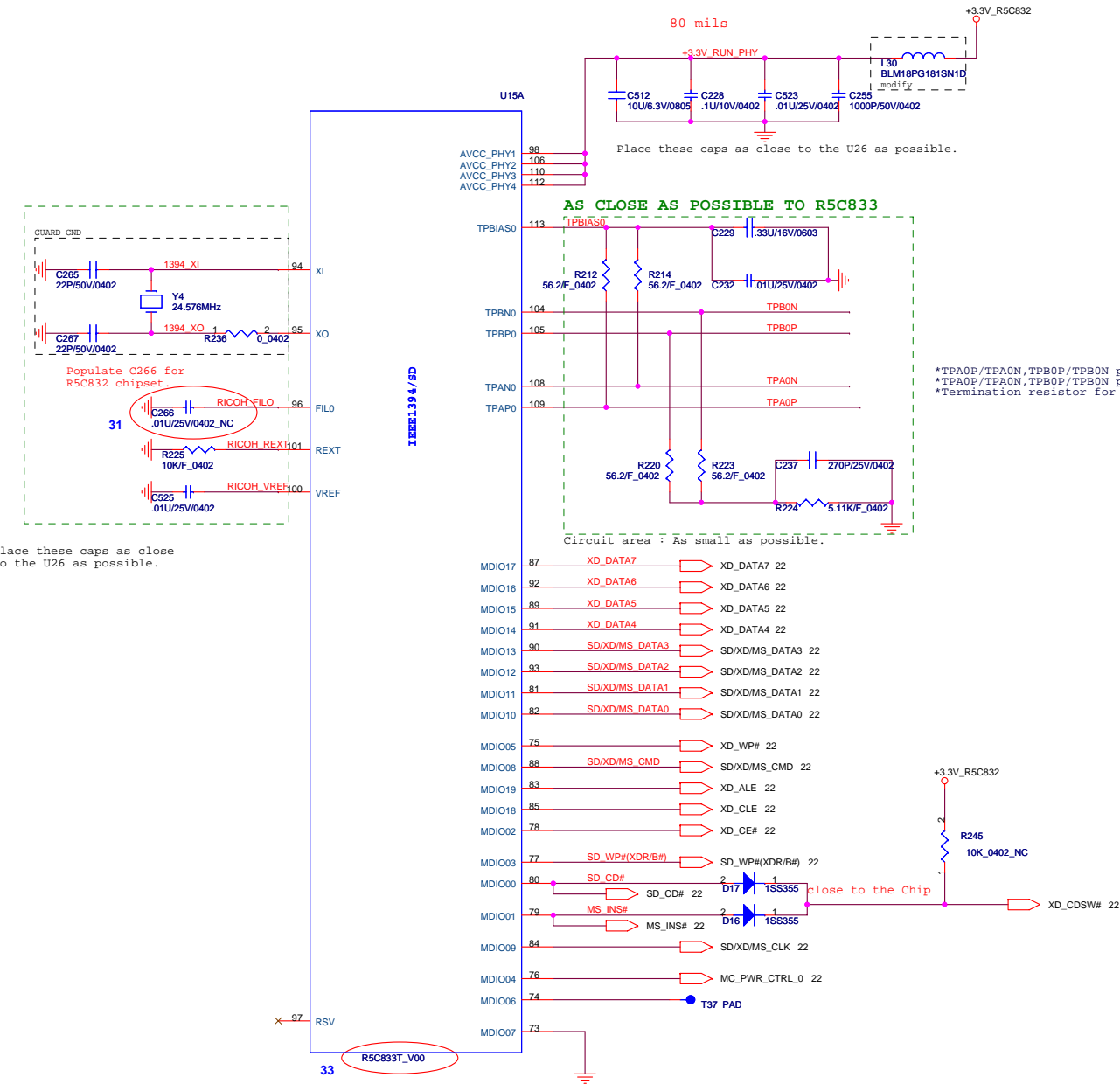


Setting R,G,B treac impedance to 50 ohm.

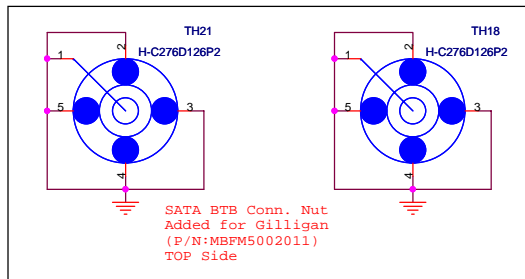
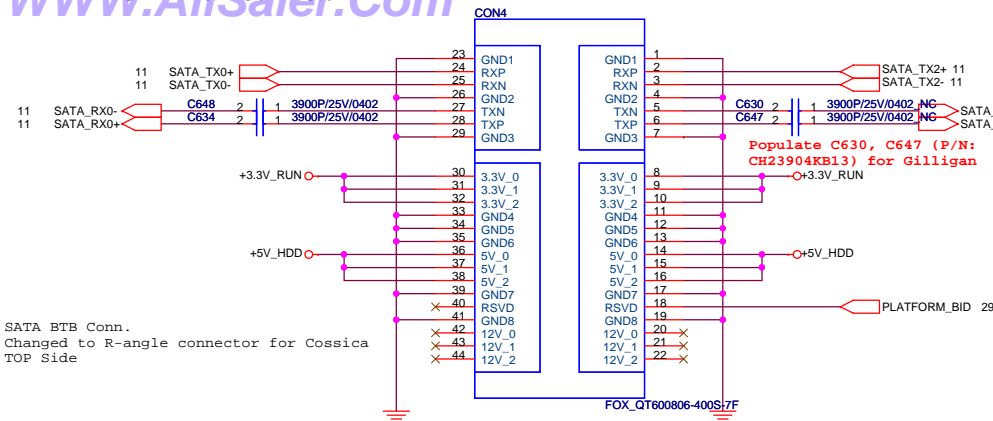


Title CRT&TV CONN		
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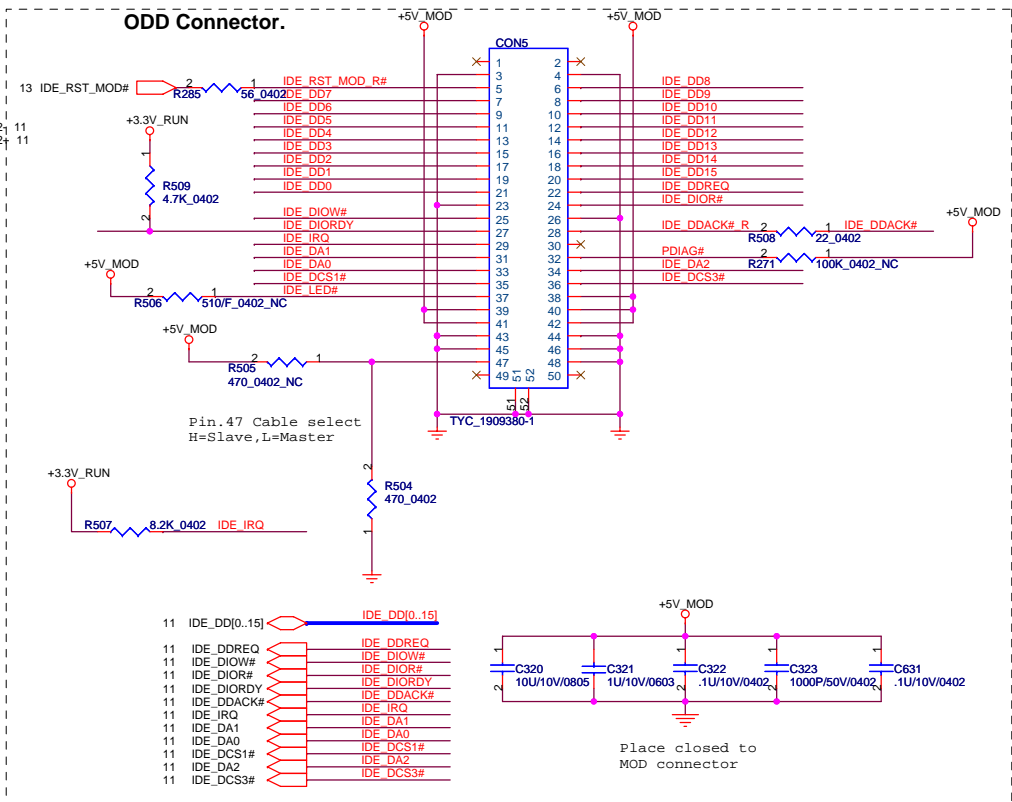




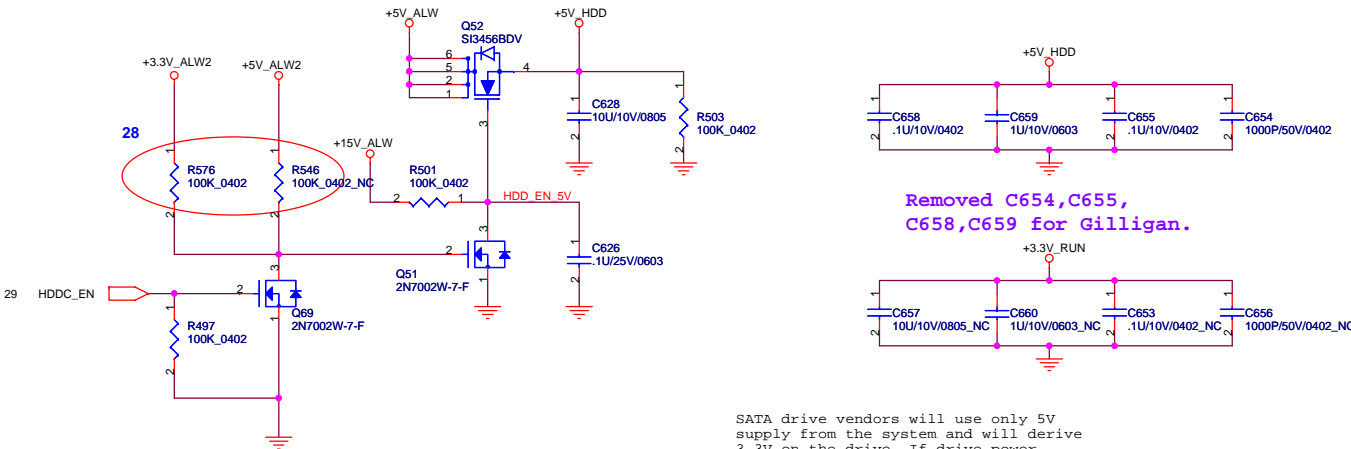
SATA 1 & 2 Connector. Change CON4 P/N to DFHS44FS611 for Gilligan.



ODD Connector.

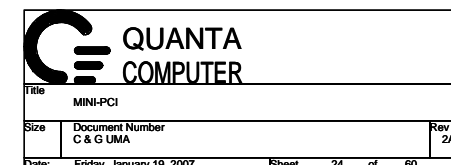


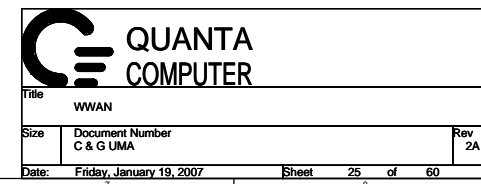
SATA 1 PWR

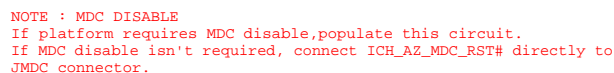
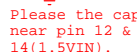
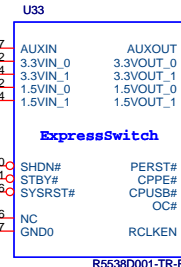
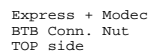
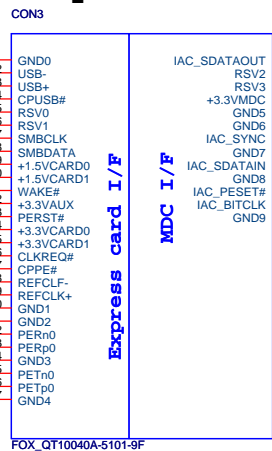


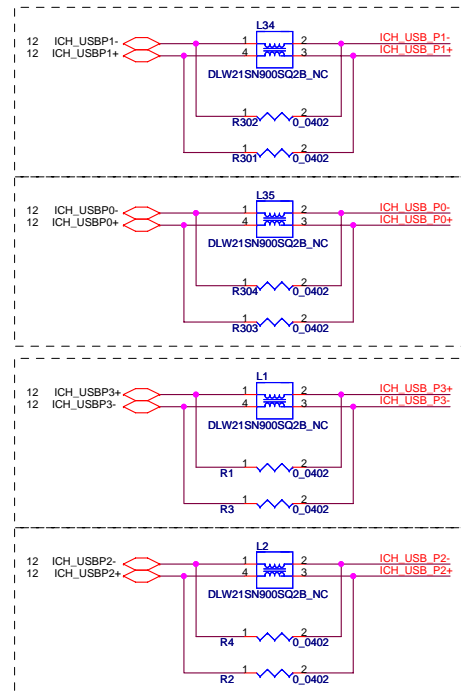
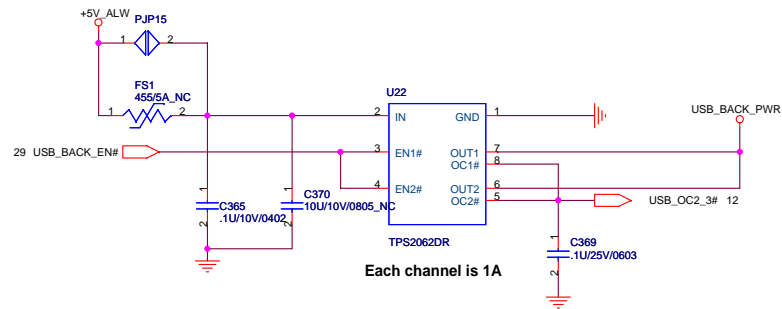
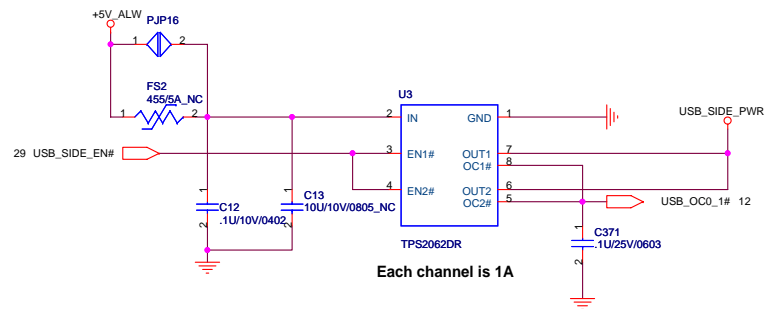
SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.

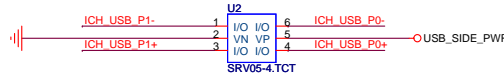




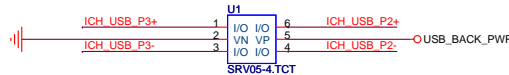




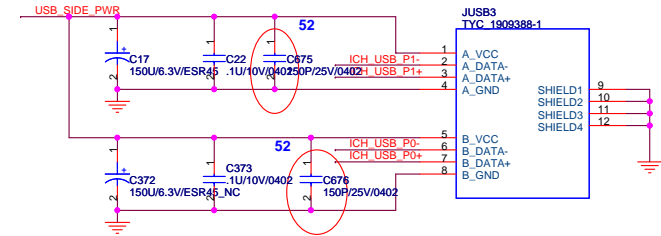
Place ESD diodes as close as USB connector.



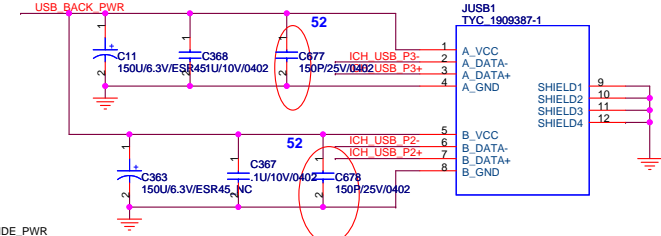
Place ESD diodes as close as USB connector.



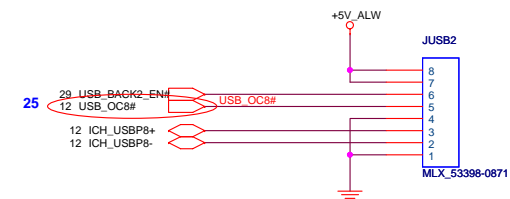
Right



Back



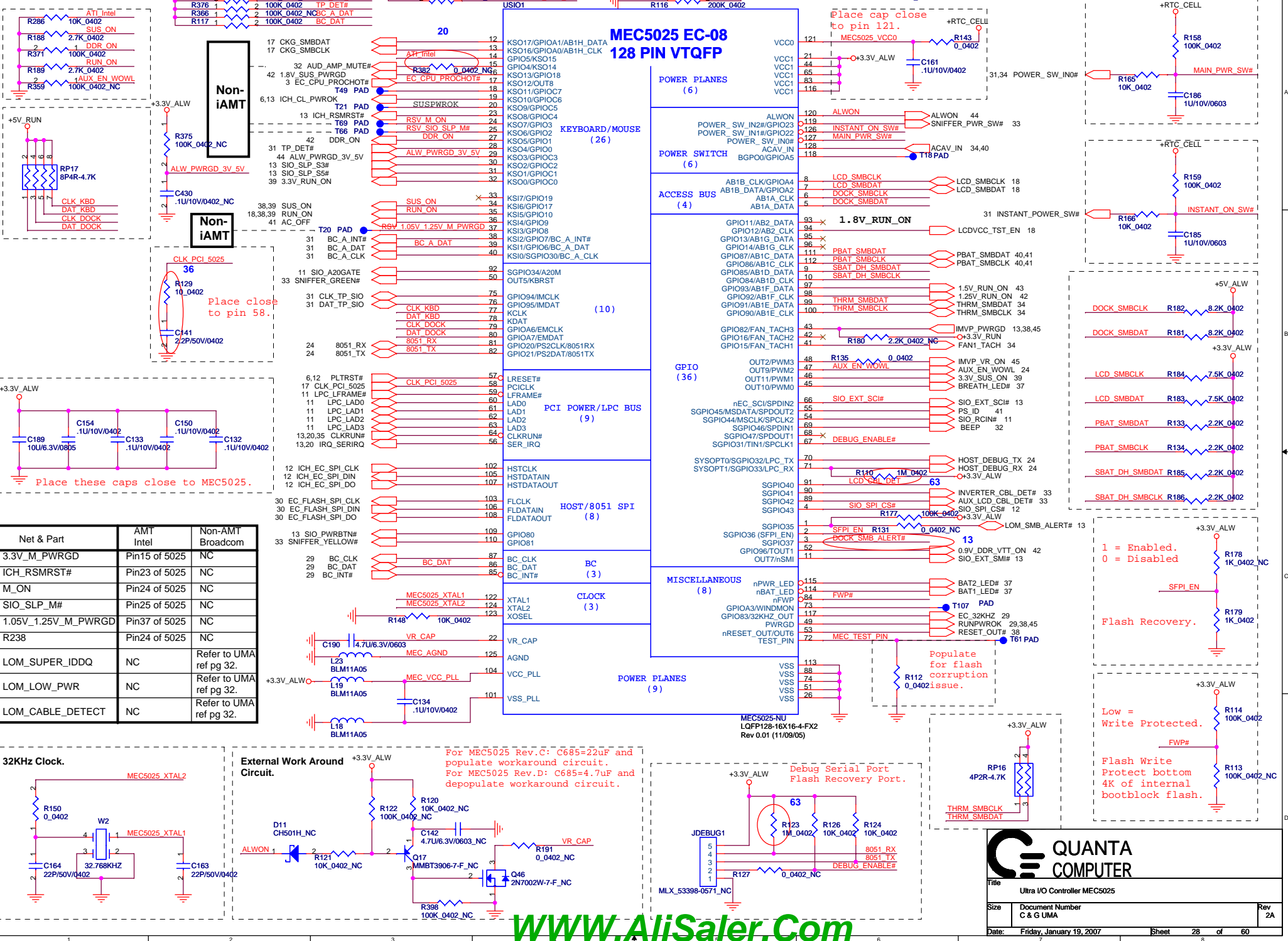
For Gilligan

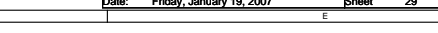
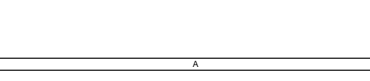


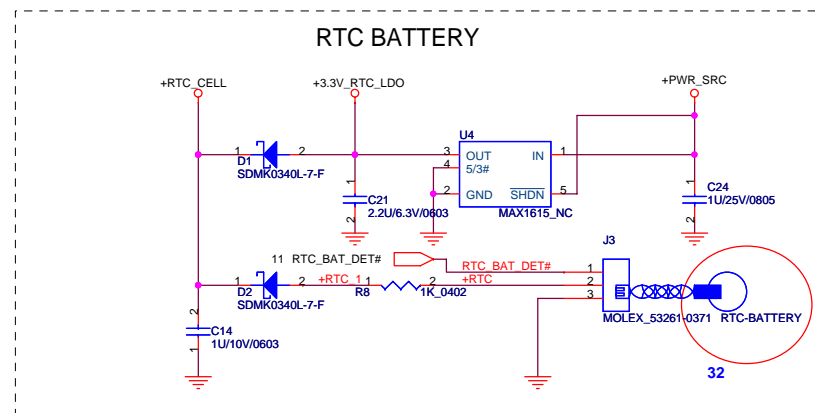
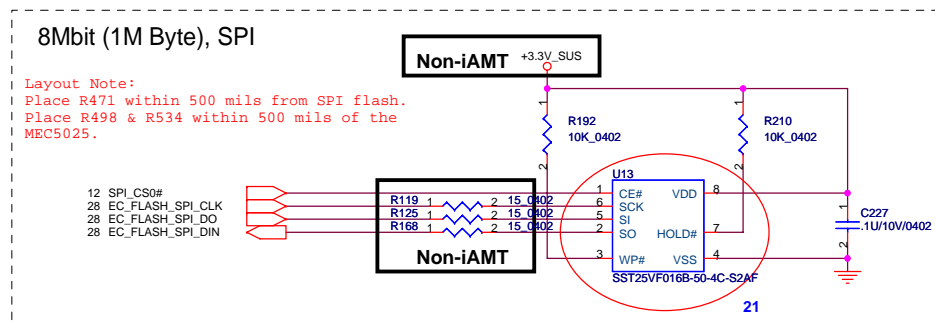
Ext. USB WTB Conn.
Populate for Gilligan
(P/N: DFHD08MS731)
TOP side

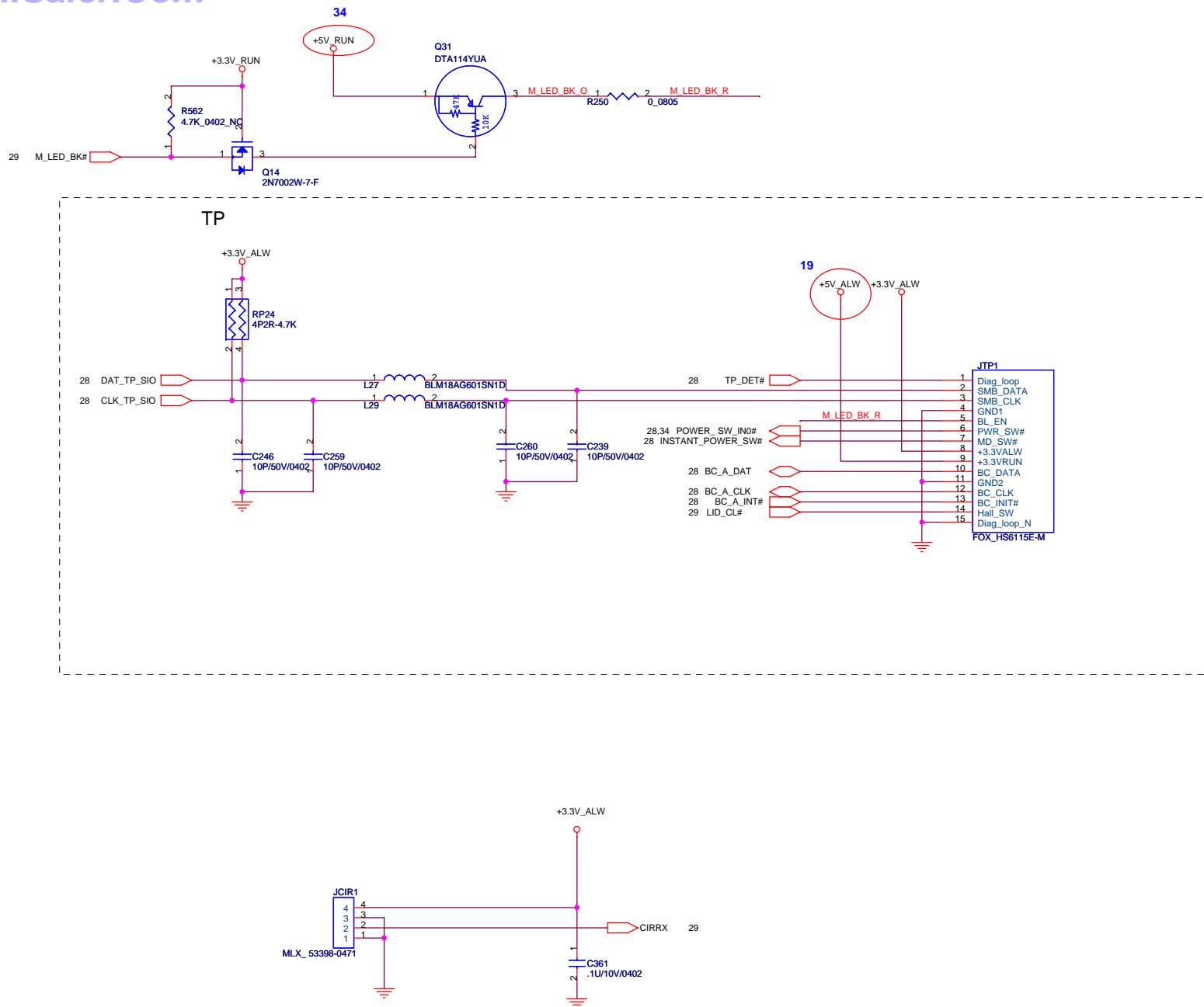


Title	External USB	Rev	2A
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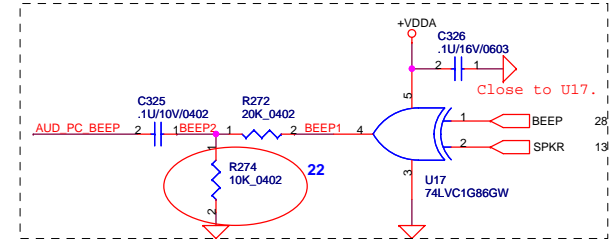
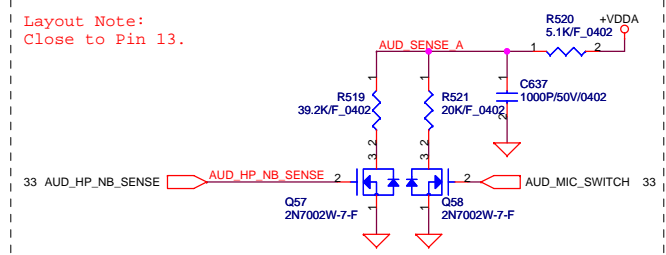
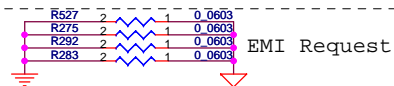
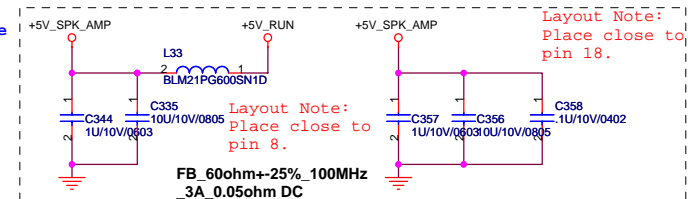
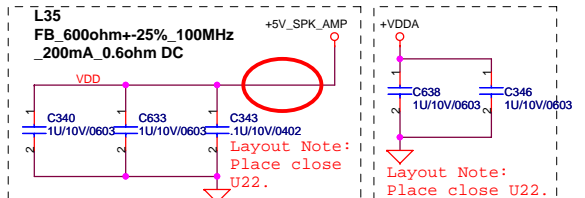
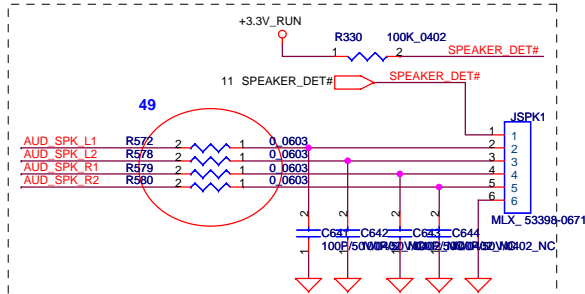
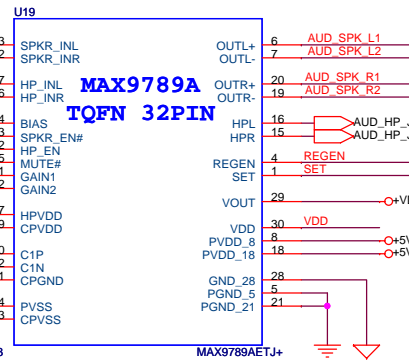




Package 1206 for THD+N performance for Vista Logo requirements.

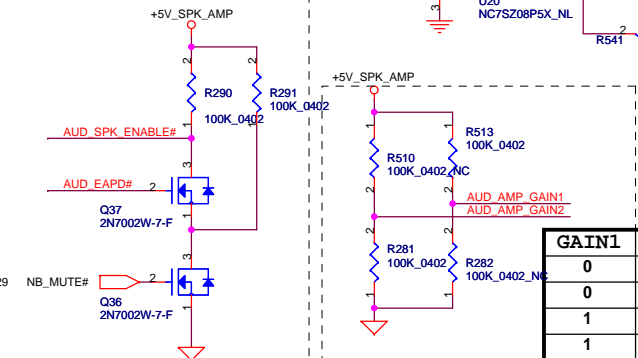
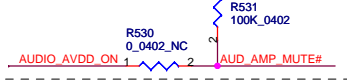
AUD LINE OUT L C331 1 2 0.033U/25V/X7R/1206
AUD LINE OUT R C332 1 2 0.033U/25V/X7R/1206
AUD HP OUT L C351 2 1 1uF/25V/X7R/1206
AUD HP OUT R C354 2 1 1uF/25V/X7R/1206

INTERNAL SPEAKER AMP



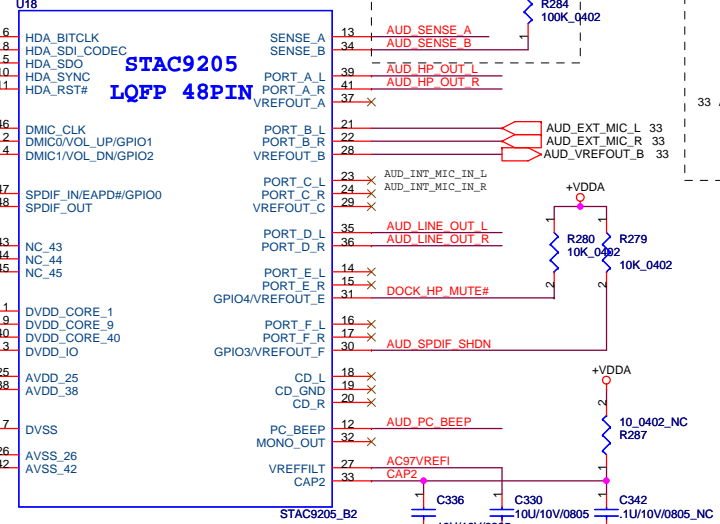
QUANTA COMPUTER		
Title Azelia CODEC(STAC9205)		
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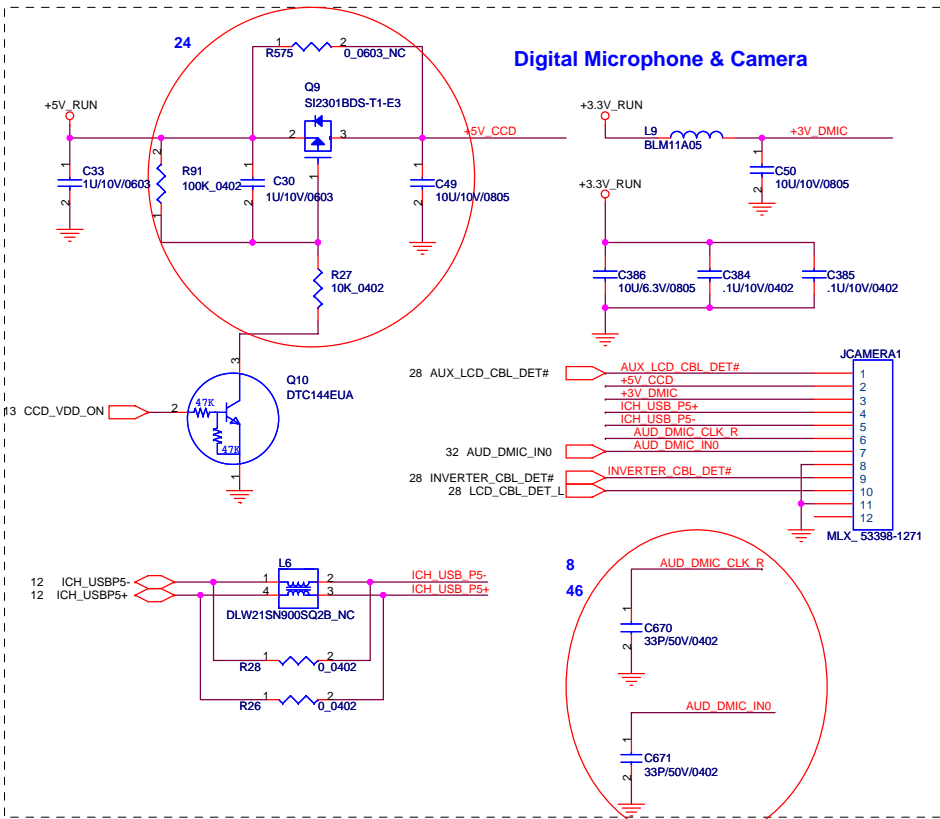
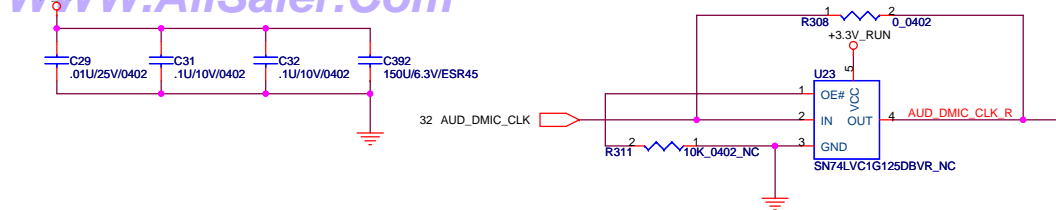
For TPA6040A, pop R530, depop R531.



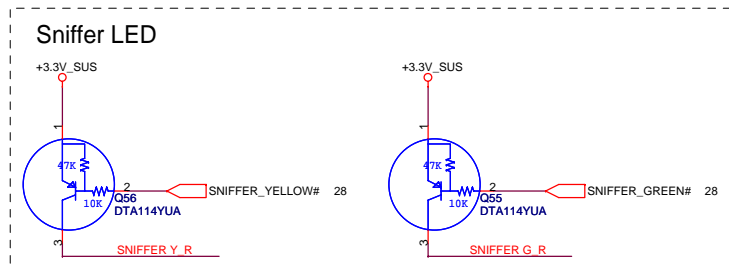
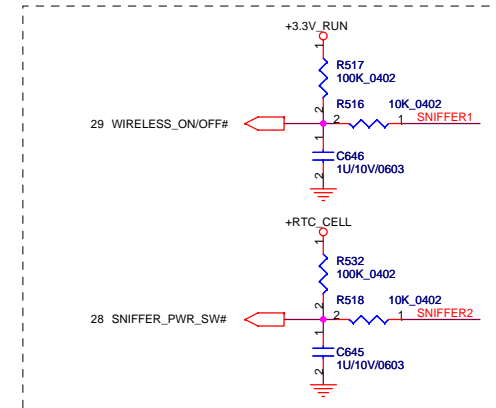
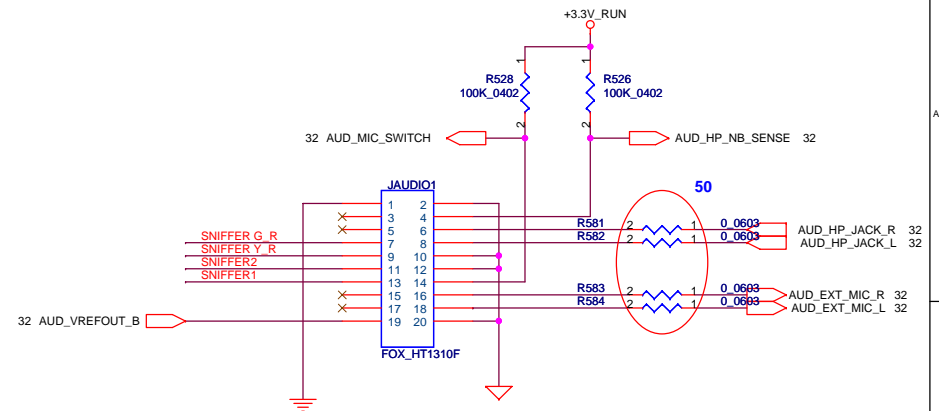
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

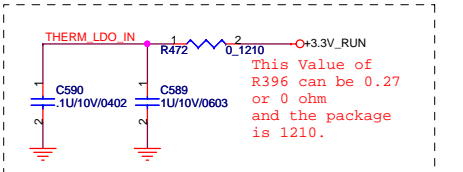
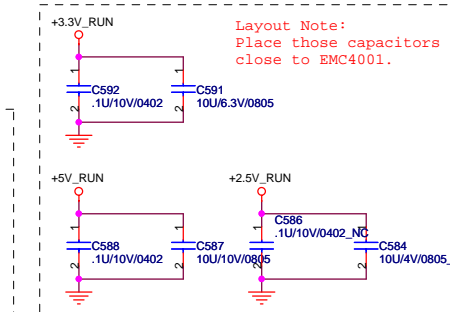
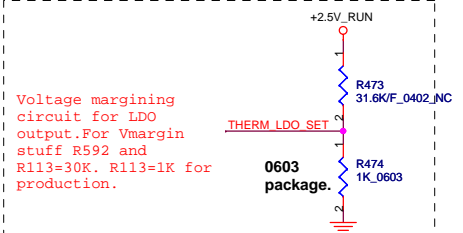
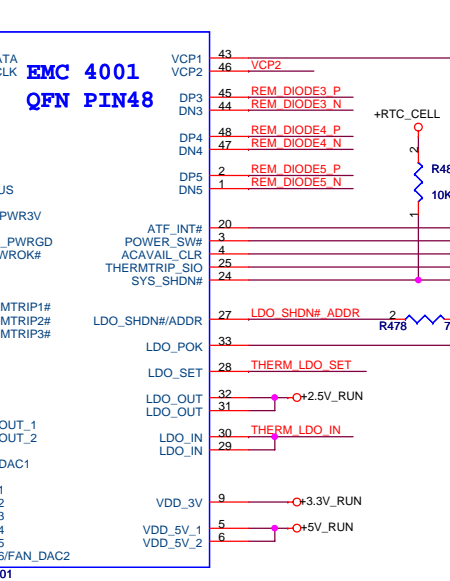
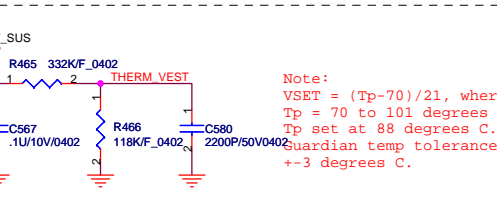
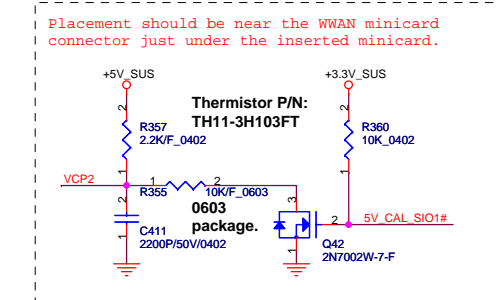
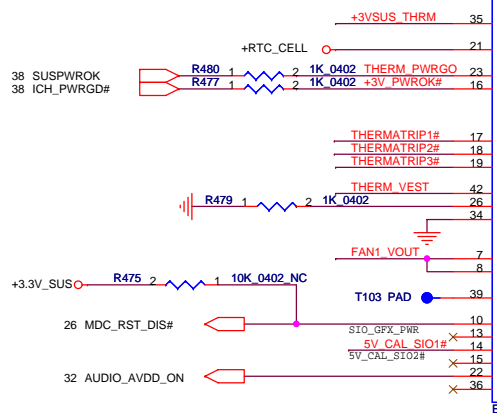
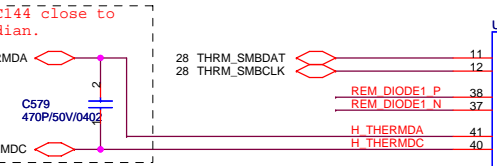
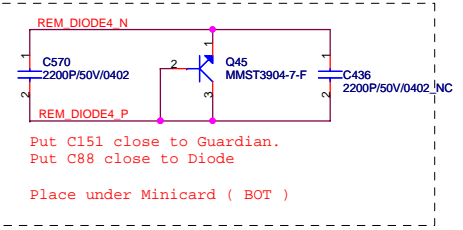
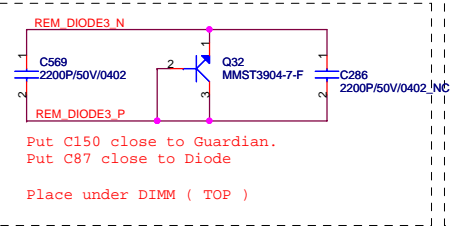
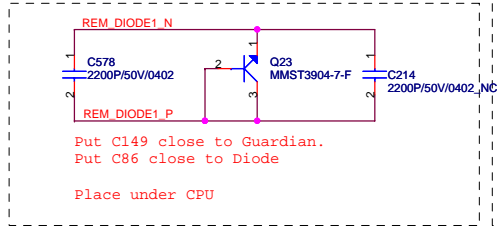
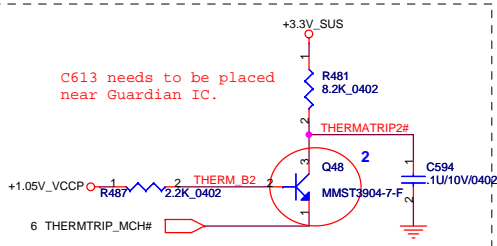
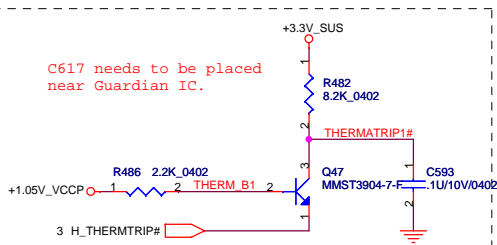
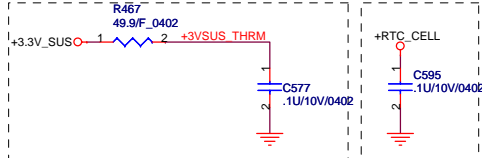
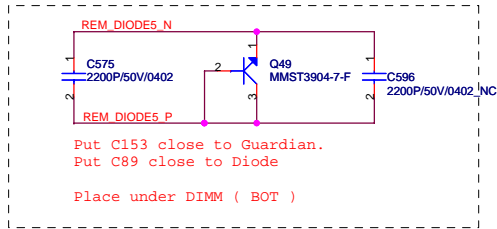
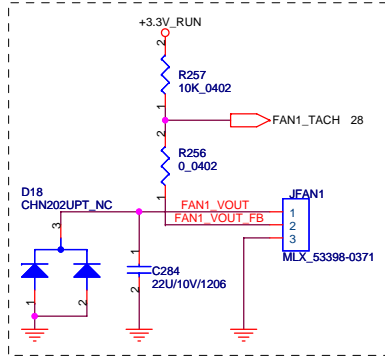
AZALIA (HD) CODEC





- | | | |
|----|------------------------------------|---------------------------------|
| 1 | Diag Loop | Diag MB connector (Local Loop) |
| 2 | Mic Signal | |
| 3 | Mic Pwr Mic Power 3.3v (run) | |
| 4 | Mic clock | Mic Clock |
| 5 | GND | |
| 6 | USB Signal | |
| 7 | USB Pwr Camera Power 3.3v (Camera) | |
| 8 | USB Clock | |
| 9 | Diag CAM | Diag Camera/Inverter |
| 10 | Diag LVDS | Diag 5v return (LVDS connector) |
| 11 | Diag Loop | Diag MB connector (Local Loop) |



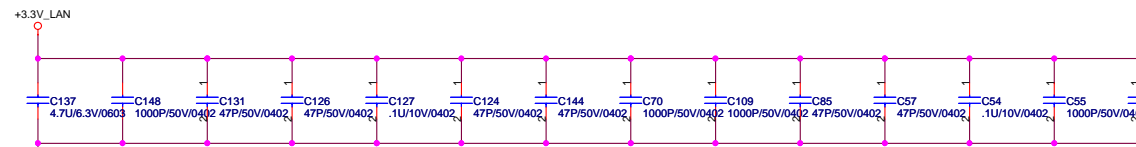


QUANTA COMPUTER

Title: FAN & THERMAL

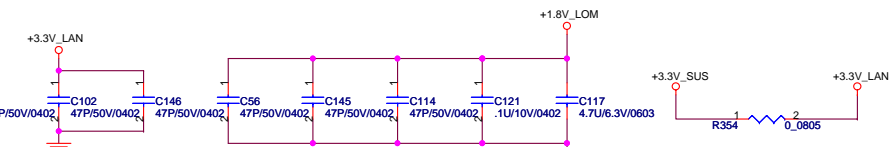
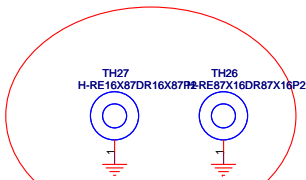
Size: Document Number C & G UMA Rev 2A

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Refer to M07_L0M4401_X06 schematic.

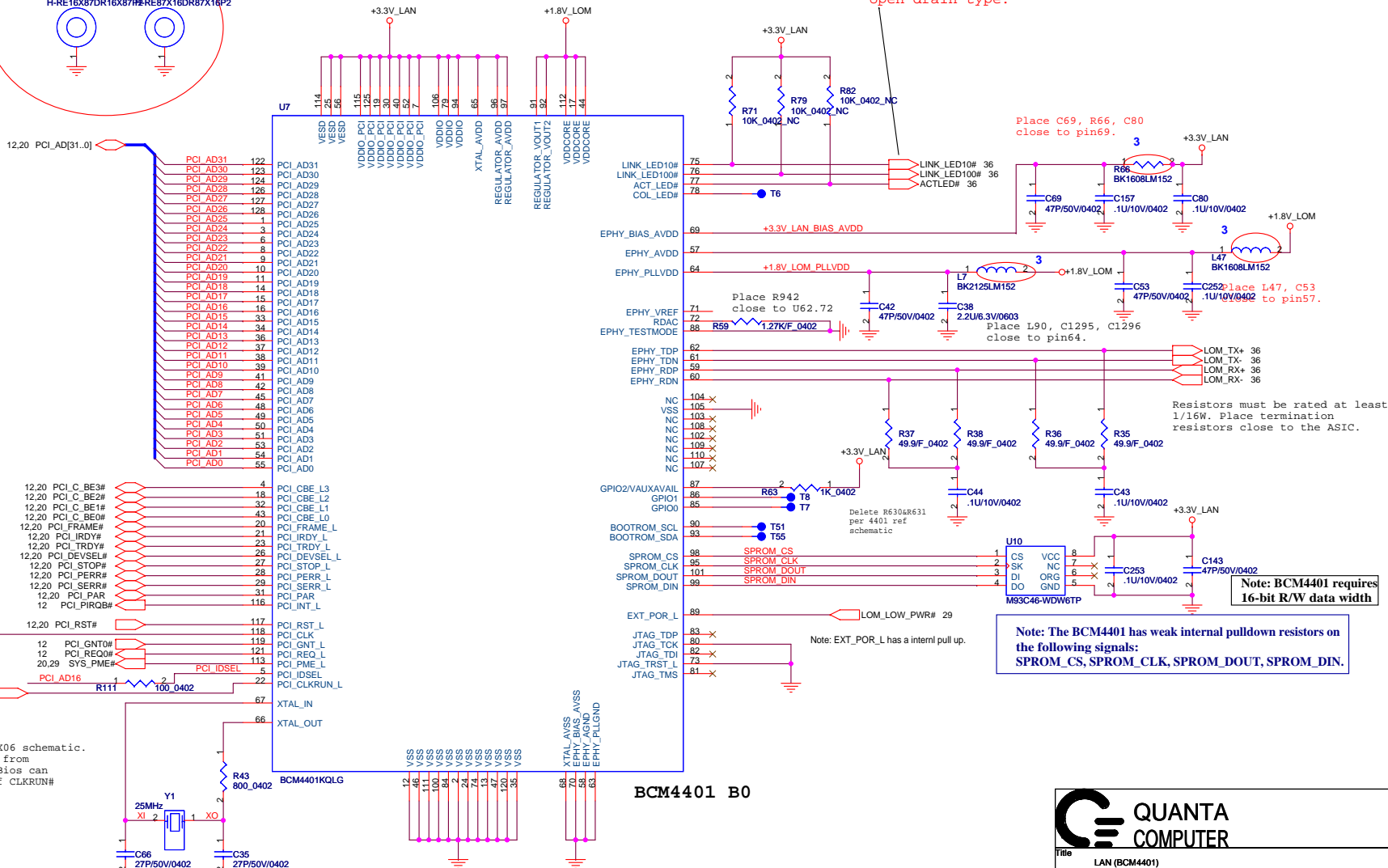
Close to power pins
0.1U*13 pcs



EMI requirement on 0812

Refer to M07_L0M4401_X06 schematic.
'+3VLAN should be sourced from
+3VSUS instead of +3VSR since WOL
is not supported on Cosica/Gilligan.

These three pin
LINK_LED10#,
LINK_LED100#,
ACT_LED are
open-drain type.



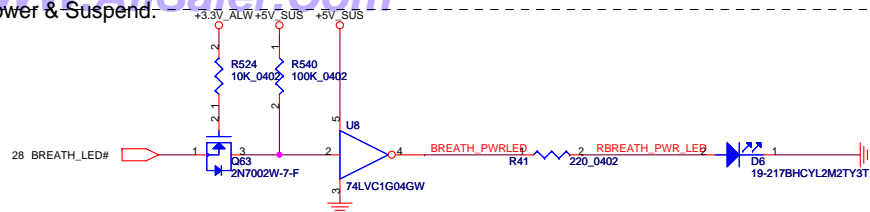
BCM4401 B0



Title			LAN (BCM4401)
Size	Document Number	Rev	
	C & G UMA	2A	
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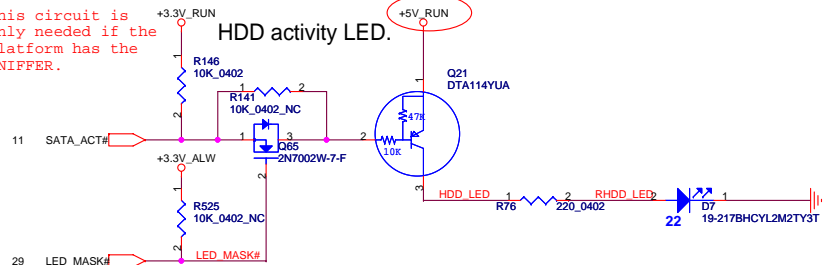


Power & Suspend:

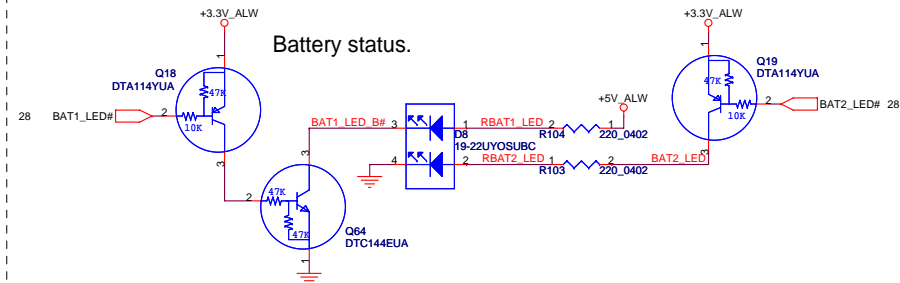


This circuit is only needed if the platform has the SNIFFER.

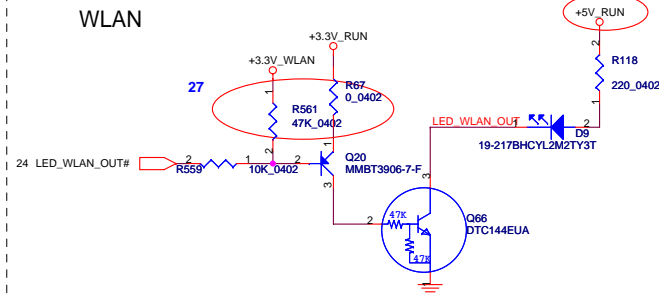
HDD activity LED.



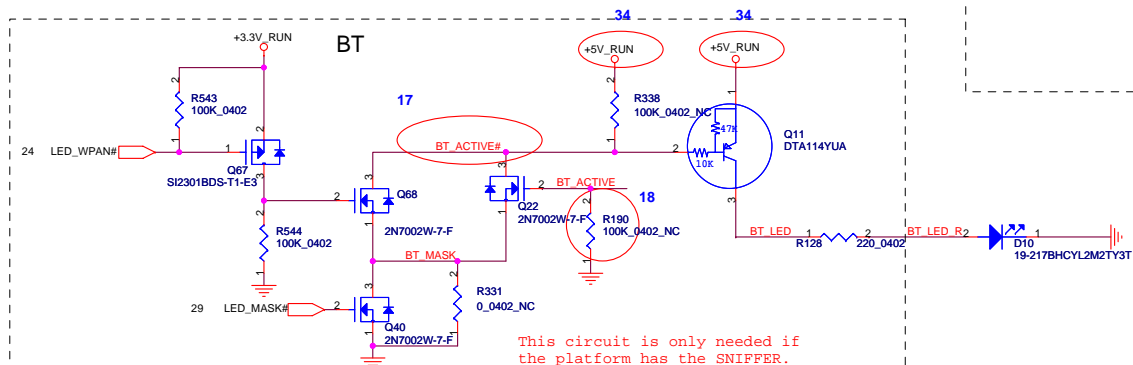
Battery status.



WLAN

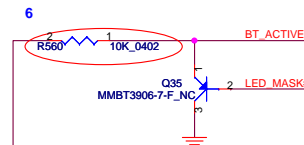


BT

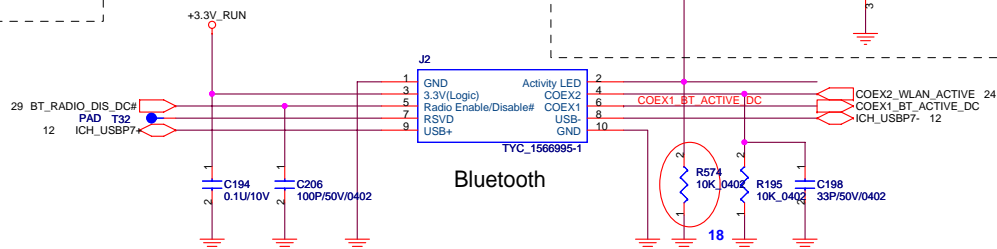


This circuit is only needed if the platform has the SNIFFER.

This circuit is only needed if the platform has the SNIFFER.



Bluetooth



SWITCH & LED

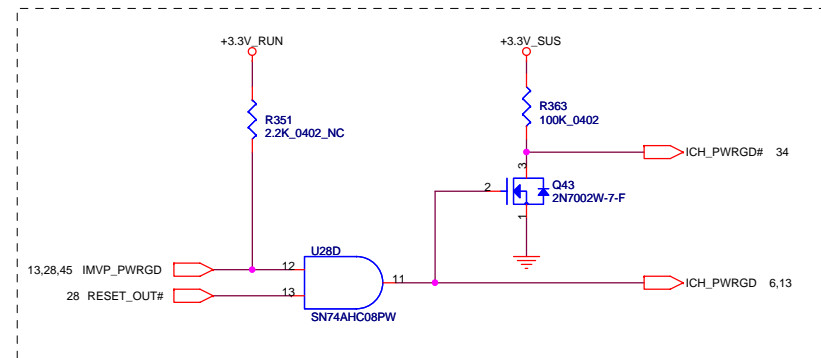
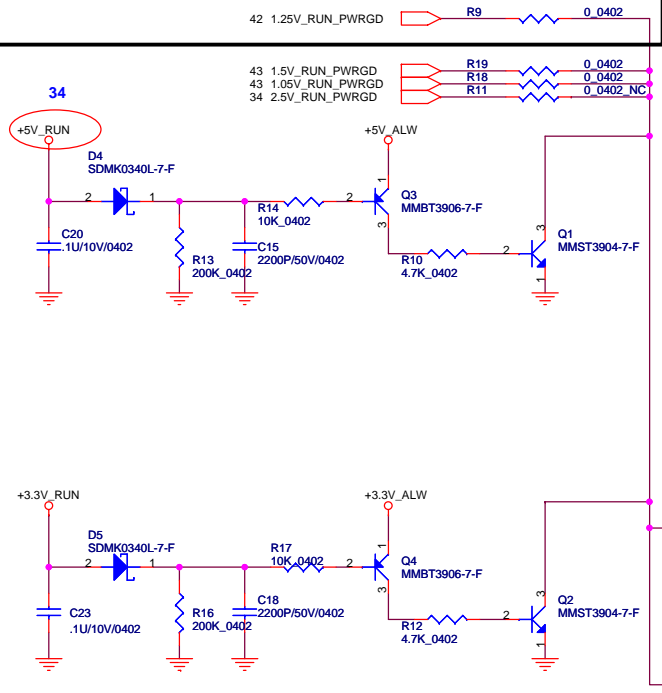
Size Document Number
C & G UMA

Date: Tuesday, January 23, 2007

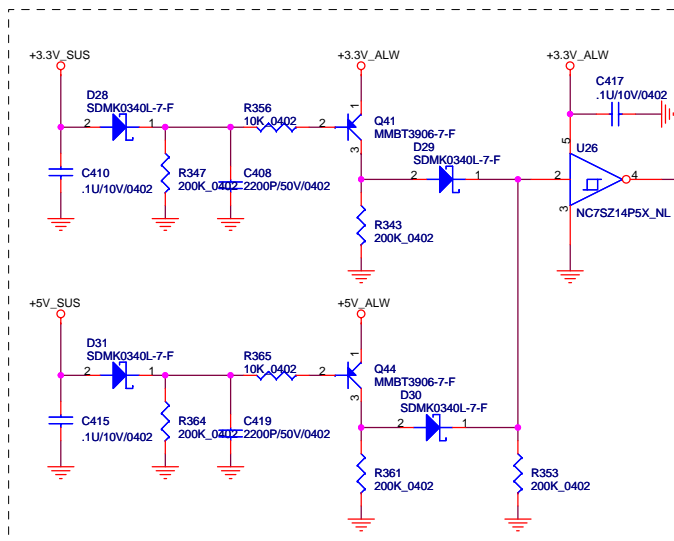
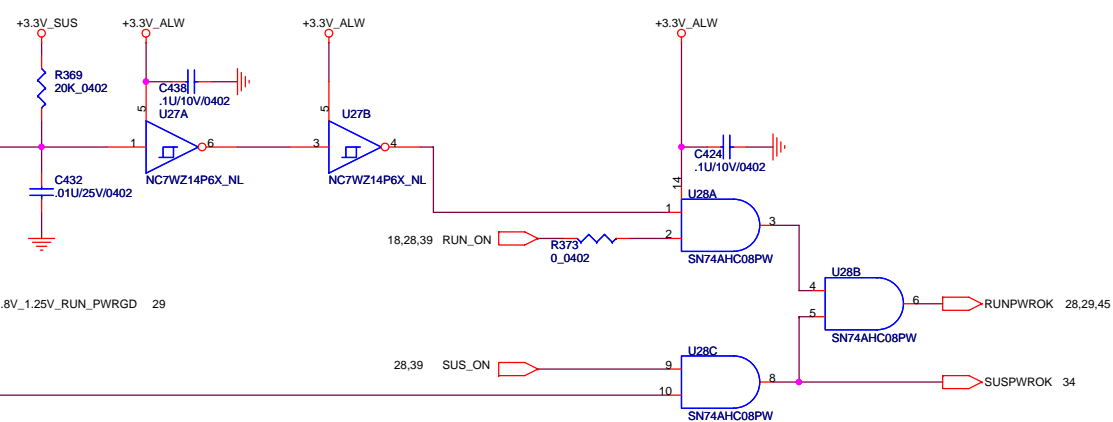
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Non-iAMT

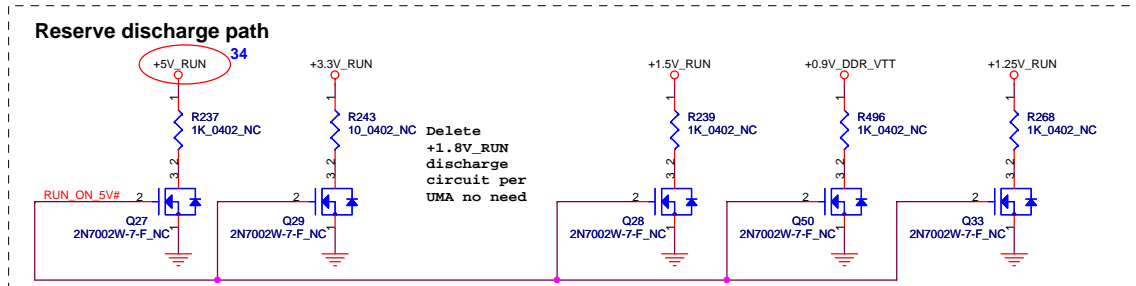
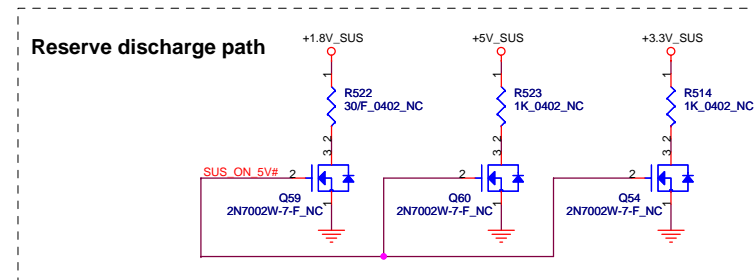
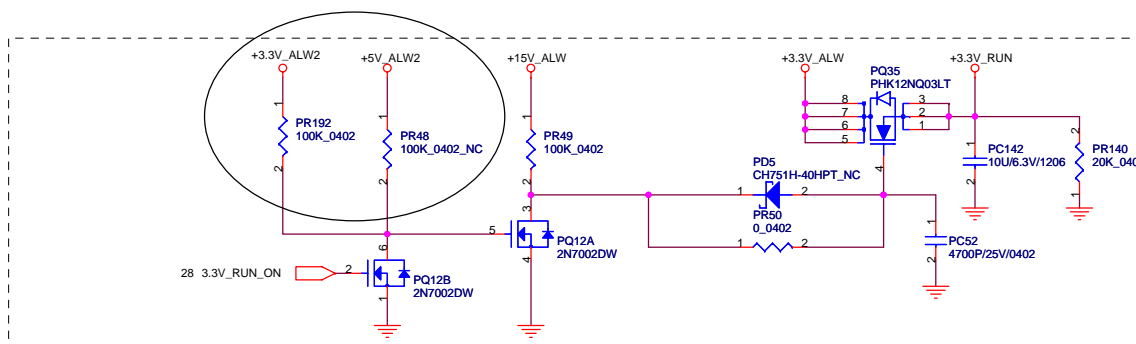
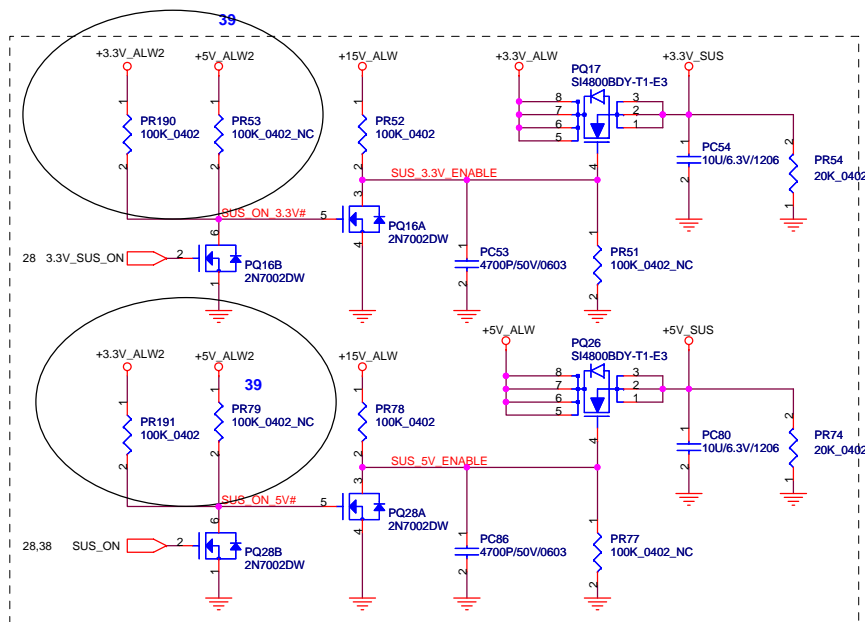
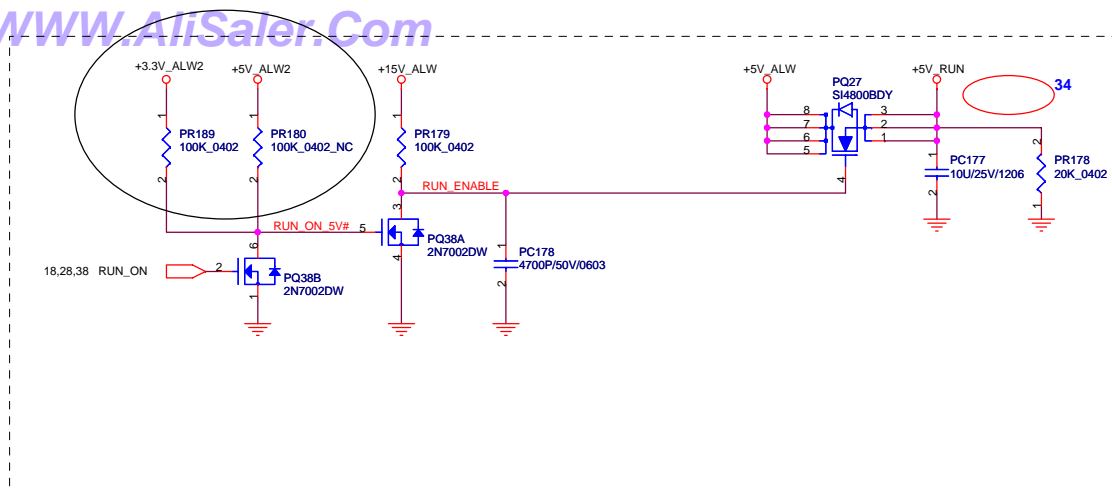


Keep Away from high speed buses



QUANTA
COMPUTER

Title System Reset Circuit		
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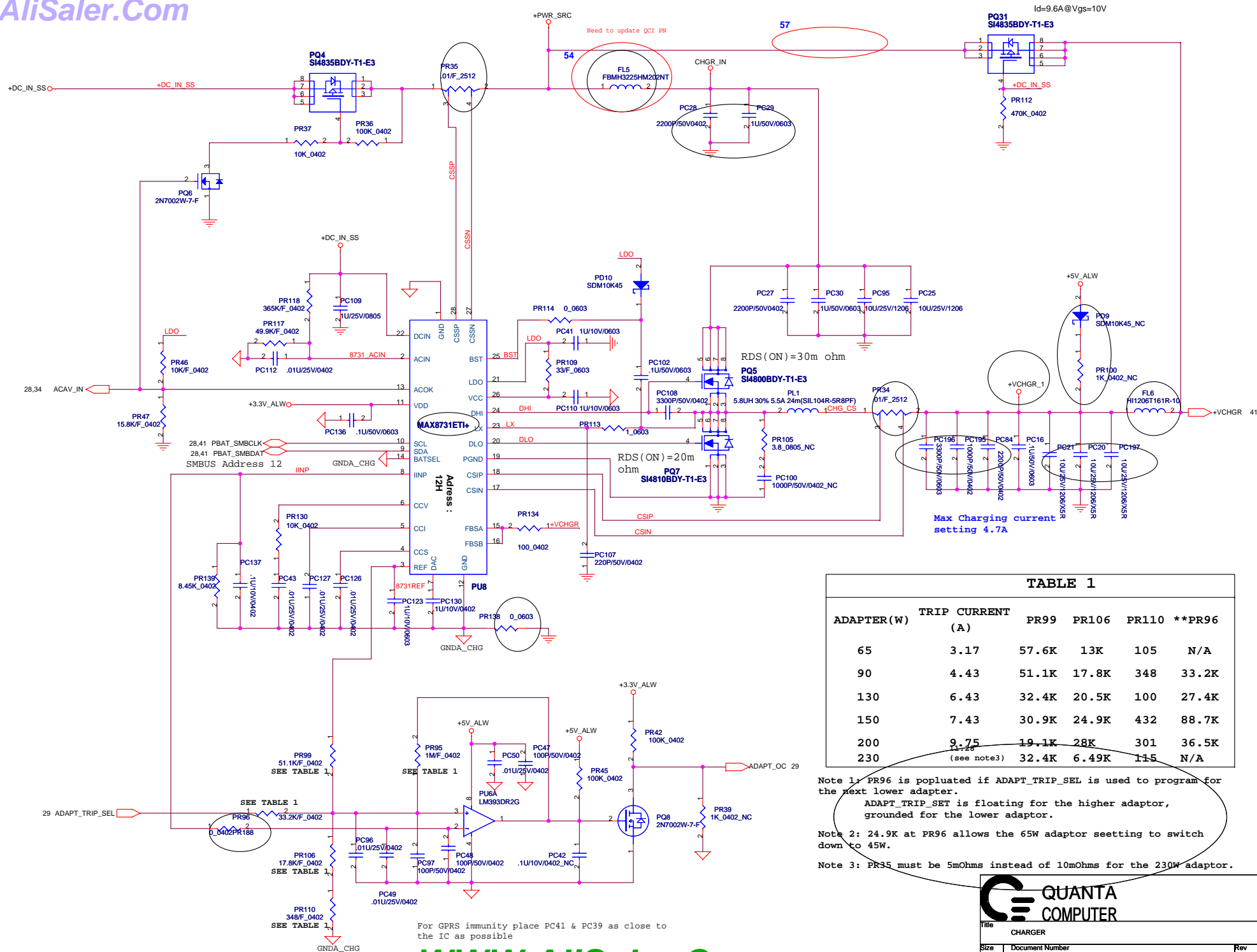


TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	PR99	PR106	PR110	**PR96
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	(see note3)	32.4K	6.49K	115	N/A

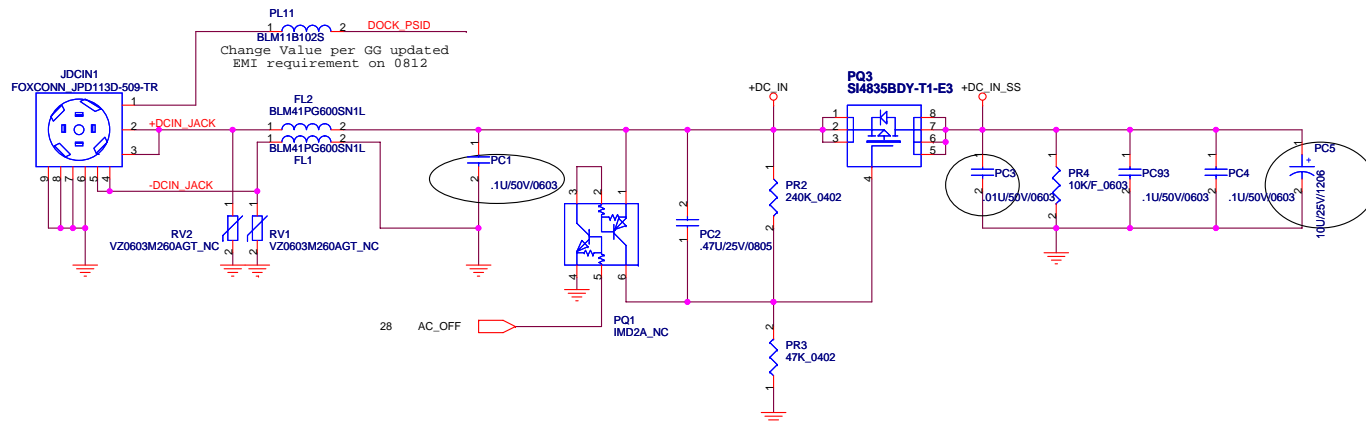
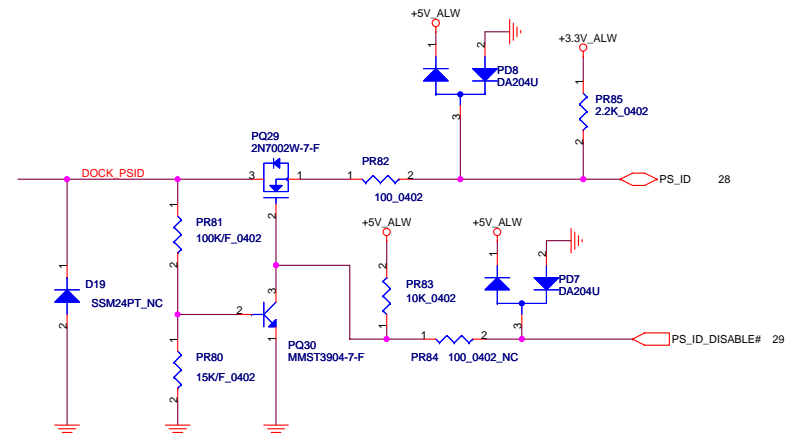
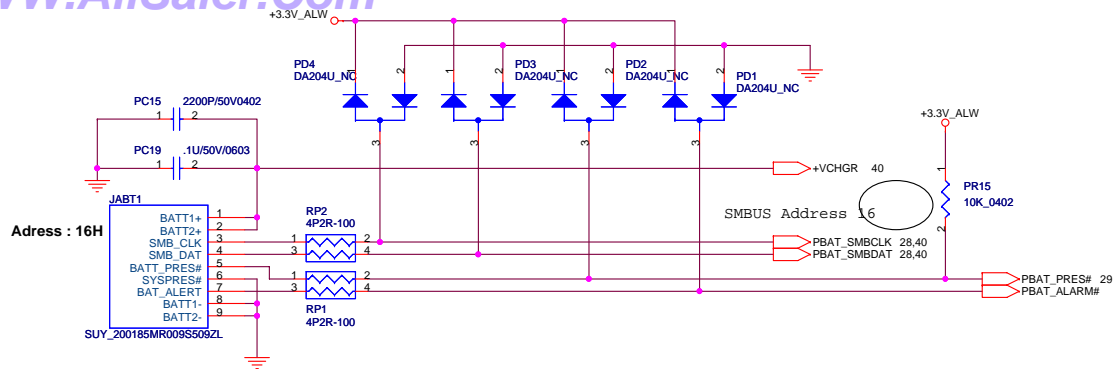
Note 1: PR96 is populated if ADAPT_TRIP_SEL is used to program for the next lower adaptor.

ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

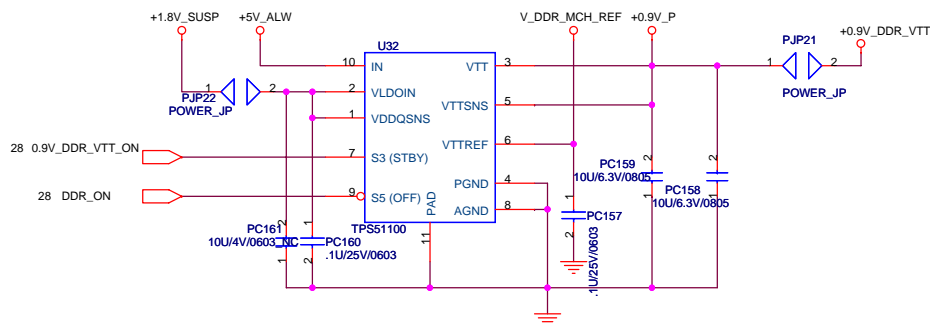
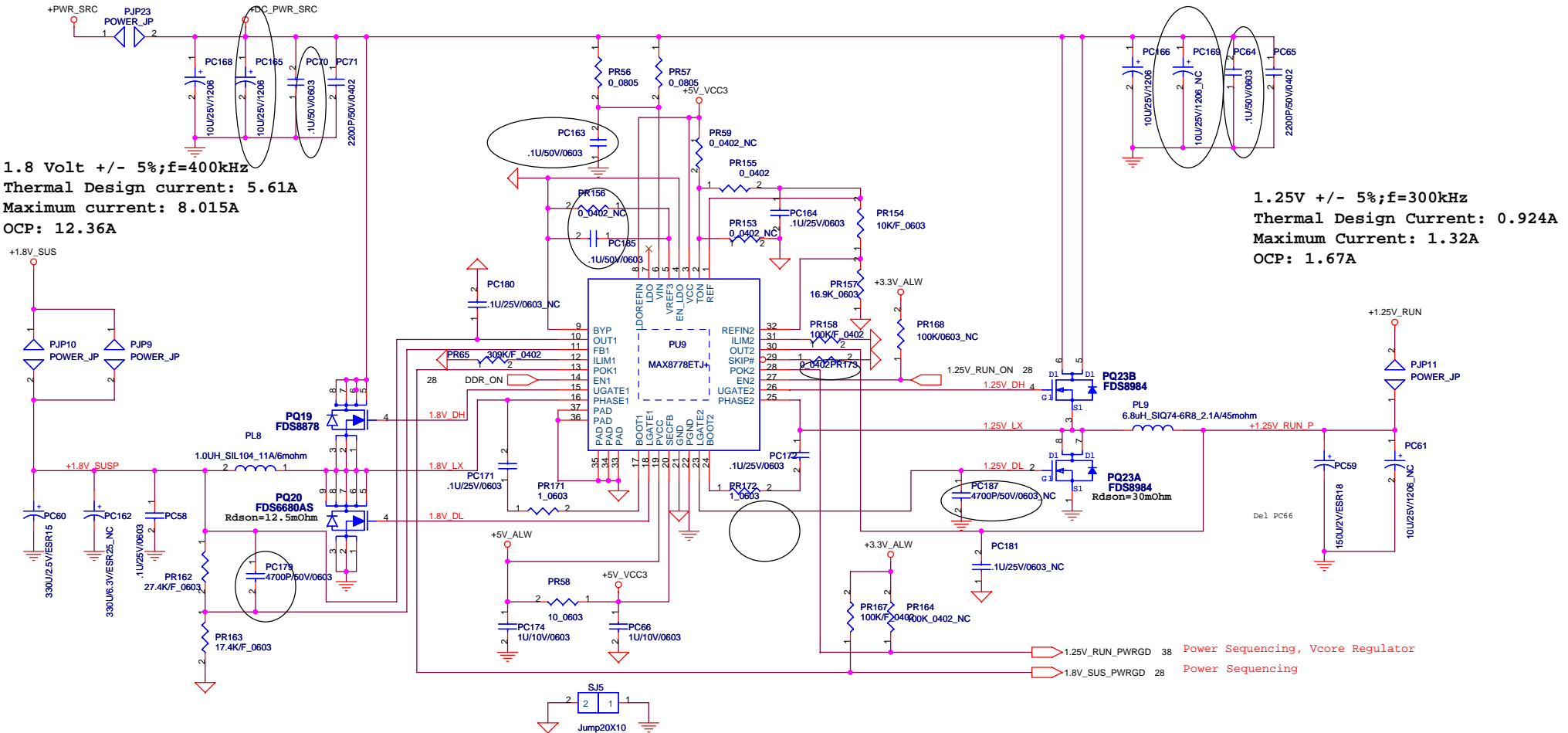
Note 2: 24.9K at PR96 allows the 65W adaptor setting to switch down to 45W.

Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.



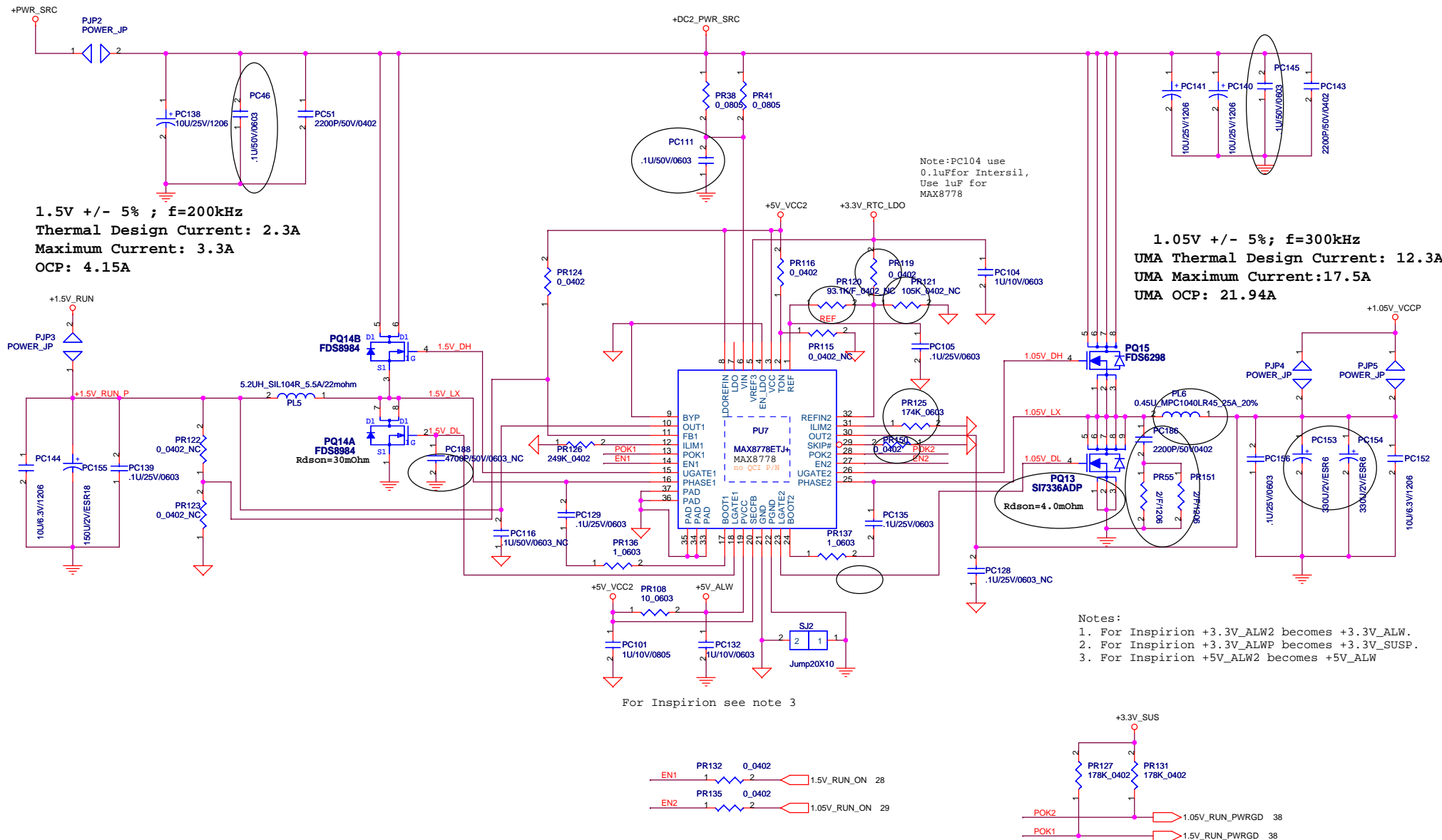


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Title DCIN,BATT CONNECTOR	
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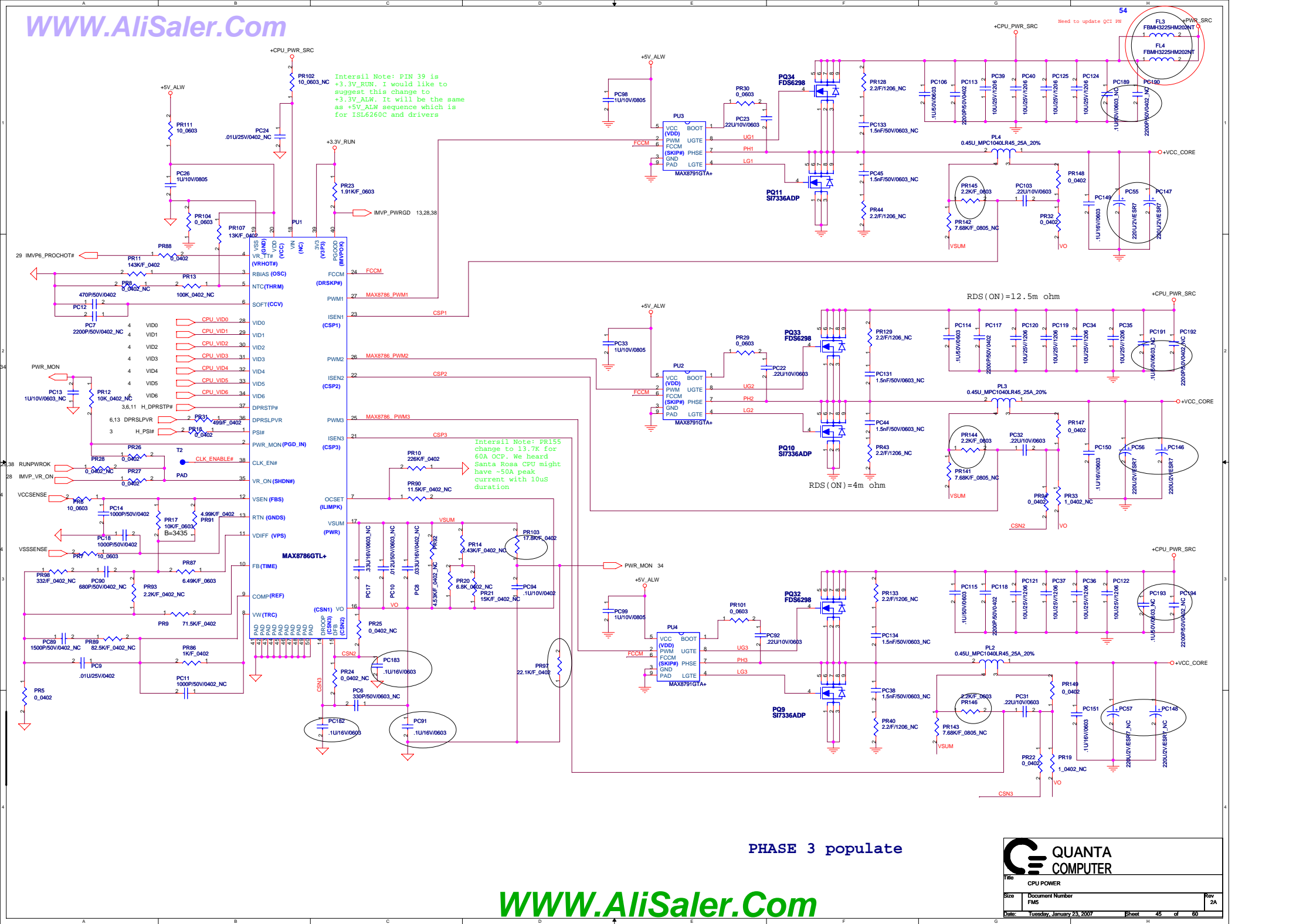


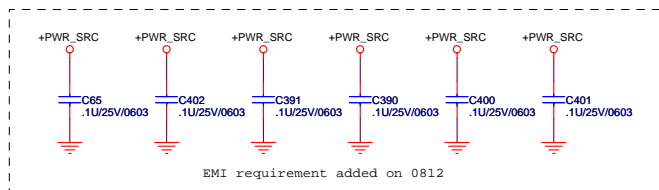
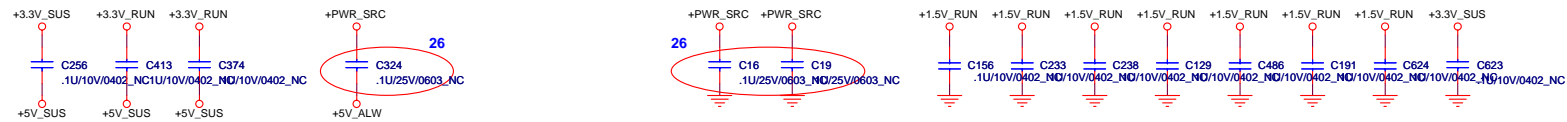
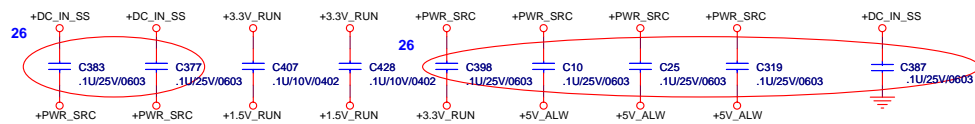
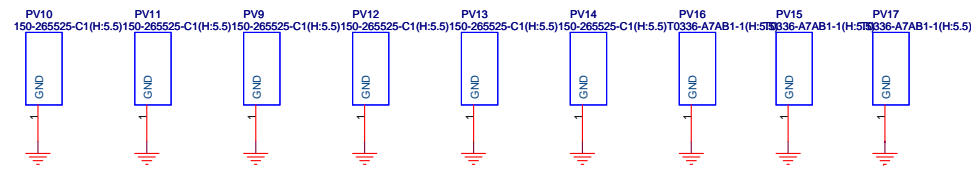
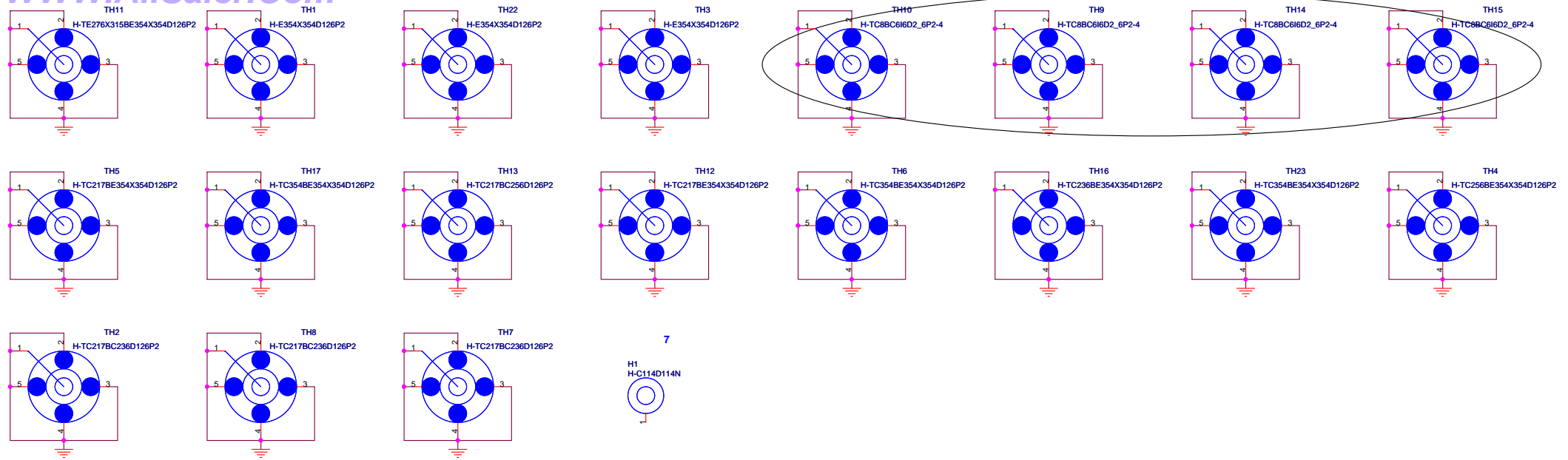
Title			1.25V, 1.05V, 1.8V, 0.9V
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+1.5V_RUN / +1.05V_VCCP / +3.3V_ALW / +3.3_RTC_LDO



Title		
1.5V,1.05V		
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Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

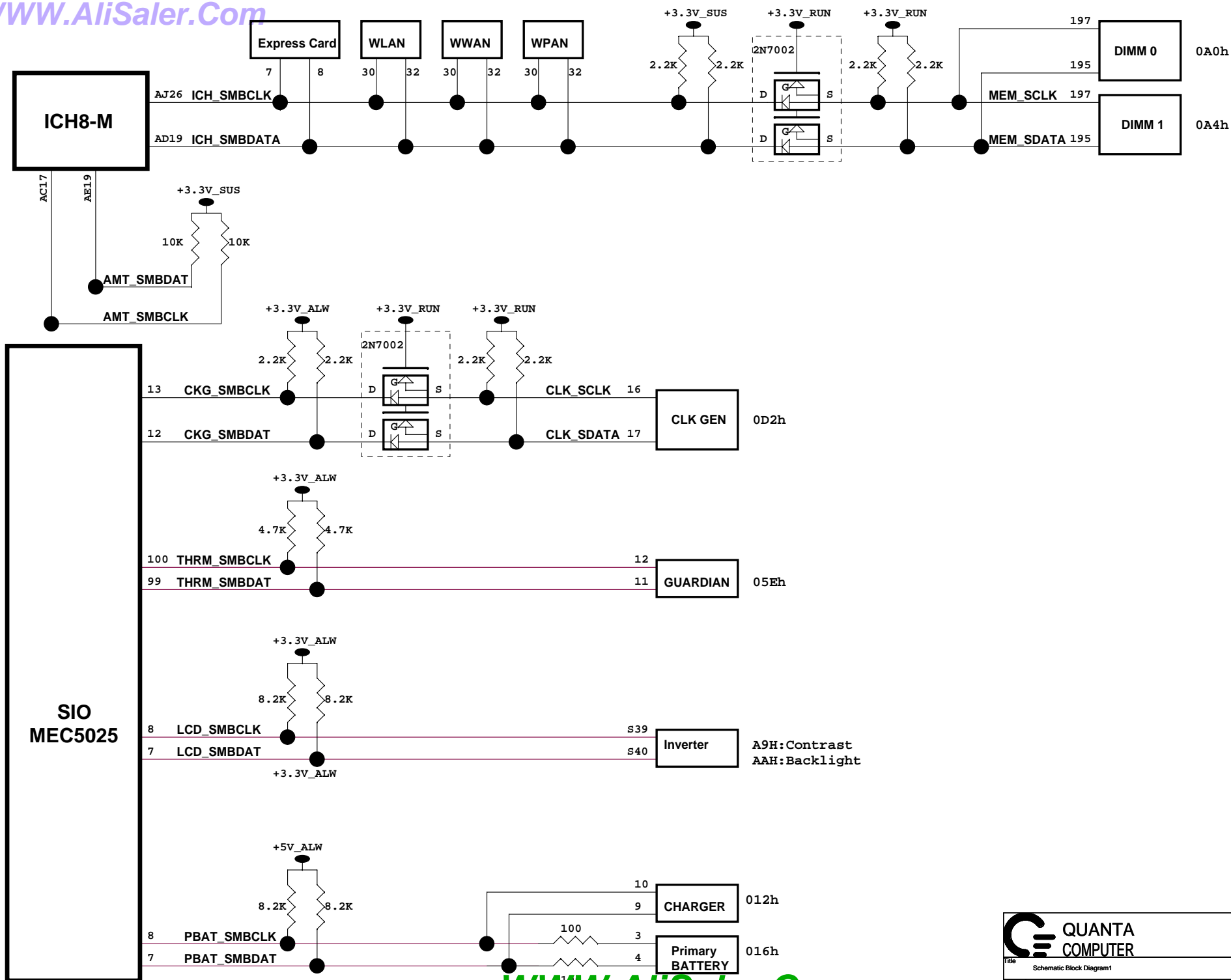
power plane State	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	OFF	ON
S5 S4/AC	ON	OFF	OFF	OFF	ON
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	ON

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
BCM4401B	AD16	REQ#0 / GNT#0	PIRQB
R5C833	AD17	REQ#1 / GNT#1	PIRQC: Card reader PIEQD: 1394

ICH8-M	USB PORT#	DESTINATION
	0	Right Top
	1	Right Bottom
	2	Side TOP
	3	Side Bottom
	4	Ext. USB TOP
	5	Digital Camera
	6	Express Card
	7	WPAN/Bluetooth
	8	Ext. USB Bottom
ECE 5011	9	WWAN
	1	None
	2	None
	3	None
	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	None



Model	Item	Page	Date	Rev.	Description
C & G UMA	1	P.3	0619	1A	Update no populated ITP schmatic per ref. Intel checklist V:1.201a. And added ITP to XDP implement txt.
	2	P.23,25,46	0620	1A	Update Screw hole per ME update.
	3	P.17	0620	1A	Update SRC CLK per followed Discrete schematic changed.
	4	P.12	0620	1A	Swap RP21.2, RP21.3, RP52.3, RP52.4, RP52.6 net for layout requirement.
	5	P.15,16	0620	1A	Swap RP14.2, RP14.4, JDIM2.136, JDIM2.137, JDIM2.141, JDIM2.143 per layout requirement.
	6	P.13,28	0620	1A	Change USIO2.28 net name from SIO_S4_STATE# to TP_DET# and delete U25.AH27.
	7	P.18	0620	1A	Update +LCDVCC circuit per ref. CD_Diag_0619.ppt file.
	8	P.33	0620	1A	Added AUX_LCD_CBL_DET#, INVERTER_CBL_DET#, LCD_CBL_DET Pull-up resistor.
	9	P.13,28	0620	1A	Delete WOL_EN of U25.AG19 and R571. Changed USIO2.94 net-name from WOL_EN to EC_ENVDD per ref BITS WI74741.
	10	P.32	0620	1A	Update JSPK1 and added SPK DET. PU Resistor.
	11	P.28	0620	1A	Delete R479 per ref BITS WI75517
	12	P.24,28	0620	1A	Added WoWL power SW circuit per ref BITS WI74552.
	13	P.6	0620	1A	Delete all of NC pins connected to test pad per ref. BITS issue WI75504.
	14	P.6	0620	1A	Populate R1, R5, R9 per implement ITP function.
	15	P.31	0621	1A	DAT_TP_SIO & CLK_TP_SIO pull up to +3.3V_ALW, Added PU to +3.3V_ALW for TP_DET#.
	16	P.33	0621	1A	Correction LCD_CBL_DET pull up circuit.
	17	P.11,30	0621	1A	Change RTC_BAT_DET# PU resistor from 10K to 100K and moved to P.30
	18	P.11,32	0621	1A	Change SPEAKER_DET# PU resistor from 10K to 100K and moved to P.32
	19	P.24,25	0621	1A	Change Mini card DET. PU resistor from 10K to 100K.
	20	P.29	0621	1A	Delete PBAT_ALERT# per M08 GPIO table removed.
	21	P.39-45	0621	1A	Update power schematic per ref power team updated schematic.
	22	P.22	0622	1A	Per TaiSol suggest, the CD2/WP2 is a dynamic pin; CD1 is a fixed pin, CD2 will touch CD1 when SD card insert into connector
	23	P.22	0622	1A	After discussion withe Taisol's FAE, pin-1 must connect to GND
	24	P.20	0622	1A	Ricoh check result: UDIO3 & UDIO4 apply NC required. Removed pull high resistor from UDIO3 and UDIO4.
	25	P.20	0622	1A	Ricoh check result: INTA# and INTB# interrupt line hange required. Please apply PCI_PIRQC# interrupt line for INTA#, PCI_PIRQD# interrupt line for INTB#
	26	P.21	0622	1A	Ricoh check result: Shield GND for XTAL for XO/XI Please apply shield GND for XTAL for XO/XI to reduce external noise for XTAL.
	27	P.12,20	0627	1A	Changed REQ2/GNT2 to REQ1/GNT1 and swap PIRQD/PIRQC for C&G card reader+1394.
	28	P.12,35	0627	1A	Changed REQ3/GNT3 to REQ0/GNT0 and change PIRQB for C&G LOM.
	29	P.35	0629	1A	L90 changed to BLM11A601.
	30	P.24,25	0629	1A	Update PCI-E chennals. Update WPAN LED signal circuit.
	31	P.23	0629	1A	Delete SATA power2 for ref. Discrete schematic.
	32	P.9	0629	1A	De-populate C1 per Intel review update.
	33	P.13	0629	1A	Delete ICH_CL_RST1# per Intel review.Delete AMT_SMBCLK & AMTSMBDAT per not support AMT function.
	34	P.39	0703	1A	Added ALW power transfer circuit per power changed.
	35	P.25	0703	1A	Change ESD2 from CDA6C05GTH to SRV05-4 per refer Dawson schematic update.
	36	P.40-45	0704	1A	Power update schematic.
	37	P.29	0705	1A	The net name of IMVP6_PROCHOT# is for pin32 not for pin33. So, I change the the net name of IMVP6_PROCHOT# from pin 33 to pin 32.
	38	P.27	0707	1A	Ref Discrete schematic, changed the pin define of JCAMERA2 between pin 5 & pin6



Title			EMI & Screw hole
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Title	EMI & Screw hole
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Size	Document Number C & G UMA
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Rev
2A

Model	Item	Page	Date	Rev.	Description
C & G UMA	1	24	9/18/2006	2A	Add SMBus isolation circuitry for WLAN.Add isolation circuitry for SMBus on WLAN.
	2	37	9/18/2006	2A	Update footprint name of D8.
	3	39- 45	9/21/2006	2A	Per Power schematic 0920, update power schematic.
	4	27	10/02/2006	2A	Update footprint name of JUSB2, and change to 8 pin.
	5	12	10/02/2006	2A	Delete ICH_USBP8+ and ICH_USBP8-
	6	19	10/02/2006	2A	Update footprint name of JVGA1.
	7	31	10/02/2006	2A	Update footprint name and QCI PN of JTP1.
	8	25	10/02/2006	2A	Update footprint name and QCI PN of JSIM1.
	9	11&23	10/16/2006	2A	Changed SATA port1 to port2 for Gilligan used.
	10	18	10/16/2006	2A	De-populate C45&C46 for LCD SMBUS rise/fall time issue.
	11	12&24	10/16/2006	2A	Update USB ports assignment
	12	18	10/16/2006	2A	Update LVDS per EMC requirement.
	13	35	10/23/2006	2A	Added L47, Change R66 to bead, Change L7 vlaue, Change C42, C69, C143, C145, C56, C114, C124, C144, C102, C126, C57, C146, C109, C70, C55, C148 pre Dell RF EMI requirement.
	14	36	10/23/2006	2A	Added L46 and changed C376 value for Dell RF EMI requirement.
	15	13	10/24/2006	2A	Change R67 value from 100K to 10K per GG list checked. Because GPIO update, Delete R67 by change item 49.
	16	34	10/24/2006	2A	Change R360 power up rail from +5V_SUS to +3.3V_SUS pwe GG updated.
	17	28 & 33	10/24/2006	2A	Per change Sniffer control same as M07 of GG list, Change Q55, Q56 from 3904 to DTA114YUA, delete R131, R132, R524, R525.
	18	28	10/24/2006	2A	Change R188&R189 value from 1M to 2.7K per GG requirement.
	19	23	10/24/2006	2A	Change HDD EN control power rail from +5V_ALW to +5V_ALW2 per GG requirement.
	20	13	10/24/2006	2A	Depopulate R329 and change R92 value from 10K to 8.2K per GG requirement.
	21	17	10/24/2006	2A	Change Single End serial damping value for fine tune value per GG requirement.
	22	11&37	10/25/2006	2A	Changed the LED control method. Move SATA LED mask to P.37. 1109 JM: Corrected LED of WLAN circuit.
	23	13	10/25/2006	2A	Depopulate R342, R352 per GG requirement.
	24	46	10/25/2006	2A	Pop C377, C407, C428, C383, C398, C10, C25, C319, C387 with 0.1uF caps for GG requirement
	25	24 & 25	10/25/2006	2A	Remove C252, C157, C253 per Mini-card no used +3V_LAN.
	26	24	10/25/2006	2A	Add R541 and non-populate for GG requirement, Changed PD on P.28
	27	24	10/25/2006	2A	Added 2 TP for GG requirement.
	28	25	10/25/2006	2A	Added R542 and non-populate per GG requirement.
	29	24 & 37	10/25/2006	2A	Moved the LED_MASK# circuit to 37 and followed GG to update BT LED control method, for this change, added R543,R544, Q67,Q68. Change Q11 from DTA114YUA to 2N7002W-7-F. Change R383 from 10K to 100K. Change R128 from 220 to 2K.
	30	24	10/25/2006	2A	Change the net of pin 5 of J4 from "COEX1_BT_ACTIVE" to "COEX1_BT_ACTIVE_Mini" per GG requirement.
	31	37	10/25/2006	2A	Change the net of pin 6 of J2 from "COEX1_BT_ACTIVE" to "COEX1_BT_ACTIVE_DC" pre GG requirement
	32	37	10/25/2006	2A	Added U34 Circuit per GG requirement.
	33	33	10/25/2006	2A	Update Audio DB BTB circuit per update connector pin define.
	35	11	10/27/2006	2A	Change CODEC bitclock with 10 ohm damping resistor per GG requirement.
	36	24	10/27/2006	2A	Added "BT_ACTIVE#" with 0_NC on J3.46 per GG requirement.
	37	17	10/27/2006	2A	Change RP10 from 33 to 10, RP3, RP5 from 33 to 22 per EA updated.
	38	17	10/27/2006	2A	Pop C71, C395, C113, C108, C104, C116 with 22p caps per GG requirement.
	39	39	10/27/2006	2A	Change +3.3V_SUS & +5V_SUS EN power up to +5V_ALW2 per GG requirement.
	40	32	10/27/2006	2A	Change C331, 332 to 0.033uF/16V/X7R/1206 & C351, C354 to 1uF/16V/X7R/1206 per Gg requirement.
	41	29	10/27/2006	2A	Depopulate EC non control resistor. Dell don't agree to do it.
	42	28	10/27/2006	2A	Depopulate EC non control resistor. Dell don't agree to do it.
	43	13&28	10/27/2006	2A	Per GPIO A14, changed U11.AG22 to LOM_SMB_ALERT#.
	44	28&29	10/27/2006	2A	Per GPIO A14, Swap DOCK_SMB_ALERT# and DOCK_SMB_PME.
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